



H61H2-AM3

Rev : A

TABLE OF CONTENTS

Page	Index	Page	Index
1	Cover Page	24	USBLAN Connector
2	Block Diagram	25	PCI Bridge IT8893 CX
3	GPIO & colay IVY Bridge map	26	Audio - ALC662 VD
4	CPU - DMI/FDI/PEG	27	Audio - CONN&HDR
5	CPU - MISC	28	USB - PWR&CONN&HDR
6	CPU - DDR3	29	SIO - IT8728 FX
7	CPU - PWR	30	FAN,COM,CASE_OPEN,THERMAL
8	CPU - GND	31	F_PANEL,BUZ,PS2,LPT
9	DDR3 - CHA DIMM1	32	DC/DC 3VDUAL,EuP
10	DDR3 - CHB DIMM1	33	DC/DC V1P05_PCH,ME/V1P8_SFR
11	DDR3 - VREF	34	DC/DC VDIMM/DDR_VTT/5VDUAL
12	PCH - DMI/PCH-PE/USB	35	DC/DC VCCSA, ATXPWR
13	PCH - SATA, SATA CONN	36	DC/DC V_CPUVTT
14	PCH - MISC, Strap Function	37	DC/DC VCORE/VAXG1
15	PCH - CLK IO,SMbus	38	DC/DC VCORE/VAXG2
16	PCH - FDI,CLR_CMOS,ROM	39	104 & STRAPPING
17	PCH - HDMI/VGA	40	Power Delivery
18	PCH - PWR	41	Power Sequence, Reset Diagram
19	PCH - GND,TCM or TPM	42	Clock Distribution
20	DVI CONN	43	XDP
21	PCIE*16,PCIE*1 Slot		
22	PCI		
23	LAN Realtek 8111E		

REVISION HISTORY:

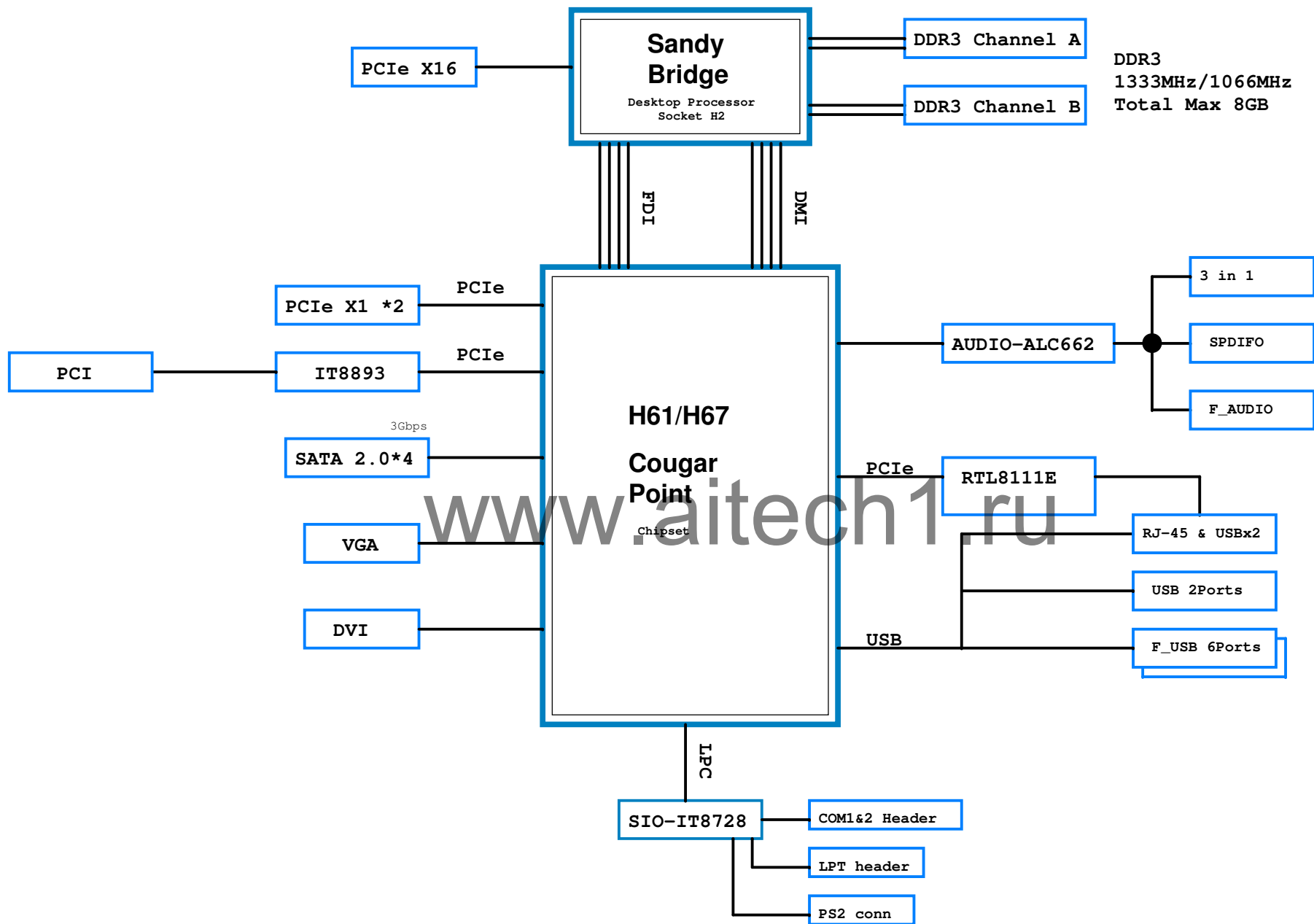
Rev	Date	Notes
V.A		

Table 1-2. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)						
	Q67	Q65	B65	Z68	H67	P67	H61
PCI Express® 2.0 Ports	8	8	8	8	8	8	6 ²
PCI Interface	Yes	Yes	Yes	No ¹⁰	No ¹⁰	No ¹⁰	No ¹⁰
USB 2.0 Ports	14	14	12 ⁶	14	14	14	10 ⁷
Total number of SATA ports	6	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁴	1 ⁵	1 ⁵	2 ⁴	2 ⁴	2 ⁴	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4	4 ⁸
HDMI/DVI/VGA/DisplayPort*/eDP*	Yes	Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP	Yes	Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	No ³
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	No
Intel® AT	Intel RST SSD Caching ¹¹	No	No	No	Yes	No	No
		Yes	Yes	No	No	No	No
Intel® AMT 7.0	Yes	No	No	No	No	No	No

- NOTES:**
1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
 2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
 3. The PCH provides hardware support for AHCI functionality when enabled by appropriate system configurations and software drivers.
 4. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
 5. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
 6. USB ports 6 and 7 are disabled.
 7. USB ports 6, 7, 12 and 13 are disabled.
 8. SATA ports 2 and 3 are disabled.
 9. PCIe ports 7 and 8 are disabled.
 10. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.1.9 for more details.
 11. Intel RST SSD Caching naming is not final at this time and is subject to change.

NOTE:
Design by
428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev2_0
443554_443554_Intel6Series_C200Series_Chipset_EDS_Rev2p0
445465_445465_Sandy_Bridge_Family_EDS_Vol2_Rev2p0



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	Case Open GPIO	GPI
GPIO1	VCC3	GPIO1_OBR	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO14	3VSB	USB_OC_L7	Native
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	R_7536_EN	GPO
GPIO34	VCC3	TP_VGA	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP_GPIO	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	R_7536_EN	Native

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	SIO_BEEP	
GP23	3VSB	Power LED	
GP22	3VSB	Power LED	
GP40	3VSB	+DIMM_5VDUAL_Control	
* GP35	VCC3	RESERVE	
* GP36	VCC3	RESERVE	
* GP37	VCC3	RESERVE	
GP47	VCC3	RESERVE	
GP14	VCC3	RESERVE	
GP66	3VSB	SMBCLK_STBY	
GP67	3VSB	SMBDATA_STBY	

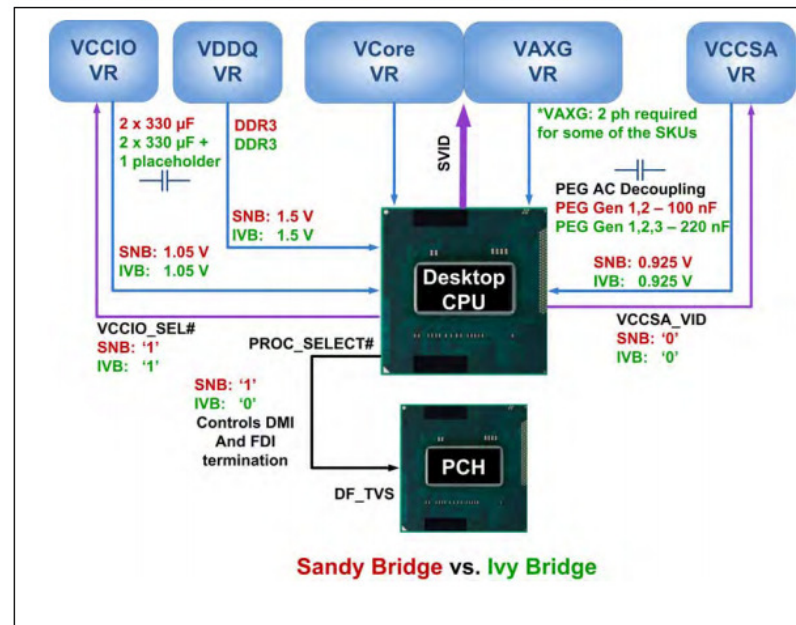
Sandy Bridge to Ivy Bridge Electrical Compatibility List

Description: The follow list provides the electrical platform deltas on designing a Desktop/Server/WS board to support both Sandy Bridge and Ivy Bridge Processors.

No	Requirement	Configuration Details	Comments
1	Processor PCI Express Graphics Guidelines	Ivy Bridge Compatible (PCIe Gen3): In order to support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 220 nF. Comply with bundle matching and fiber weave as specified in the Rev1.5 PDG. Sandy Bridge only implementation: The AC coupling caps are of value 75-200nF to support Gen1 and Gen2 PCIe.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 4.1.7: Table 4.4
2	DDR3 VREF	Ivy Bridge Compatible: Route DIMM VREFA and DIMM VREFB from the CPU to the DIMM Write VREF circuit. Sandy Bridge only implementation: The DIMM VREFA and DIMM VREFB pins from the CPU do not need to connect to the DIMM write VREF circuit.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 3.4
3	PROC_SELECT# and DF_TVS Signals	Ivy Bridge Compatible: Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 4.7K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH V_NAND_IO rail. Sandy Bridge only implementation: PROC_SELECT# can be left as No Connect or same as IVB connectivity. DF_TVS needs to be pulled up to V_NAND_IO power rail through 2.2 K Ohm +/-5% resistor.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 5.4.4, Figure 5-4
4	VCCIO VR Implementation	Ivy Bridge Compatible: Need to design your VR to be 1.0/1.05V selectable via the VCCIO_SEL pin. No additional VRs needed for compatibility Sandy Bridge only implementation: VCCIO VR can be fixed at 1.05V	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9
5	VCCSA VR implementation	Ivy Bridge Compatible: Design your VR to be 0.925/0.85V selectable via VCCSA_VID0 pin. Sandy Bridge only implementation: VCCSA VR can be fixed at 0.925 V.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9

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Figure 1-2. Desktop Sandy Bridge vs. Ivy Bridge Compatibility Diagram

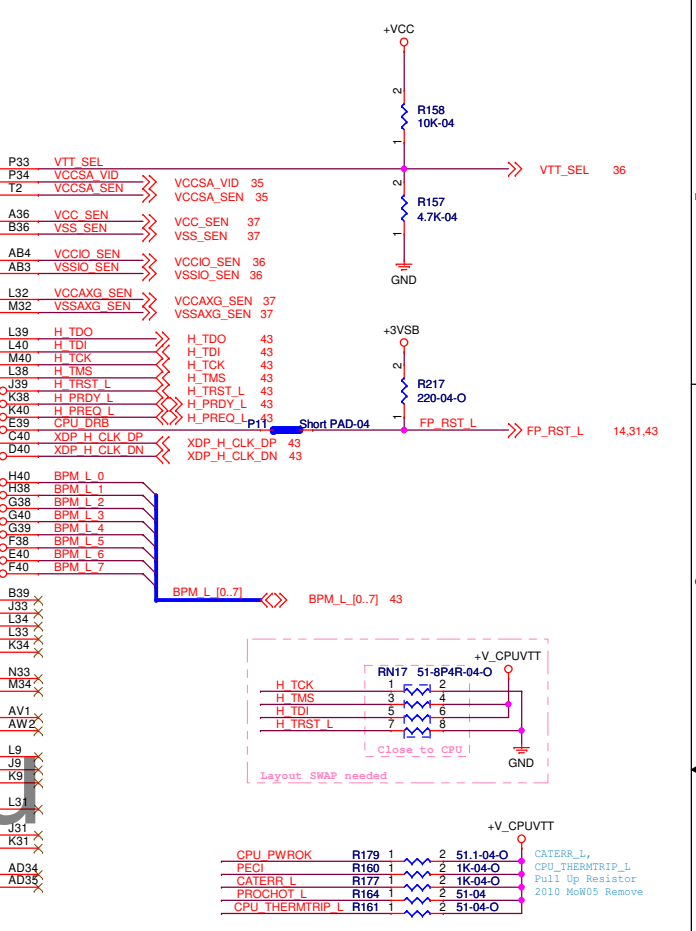
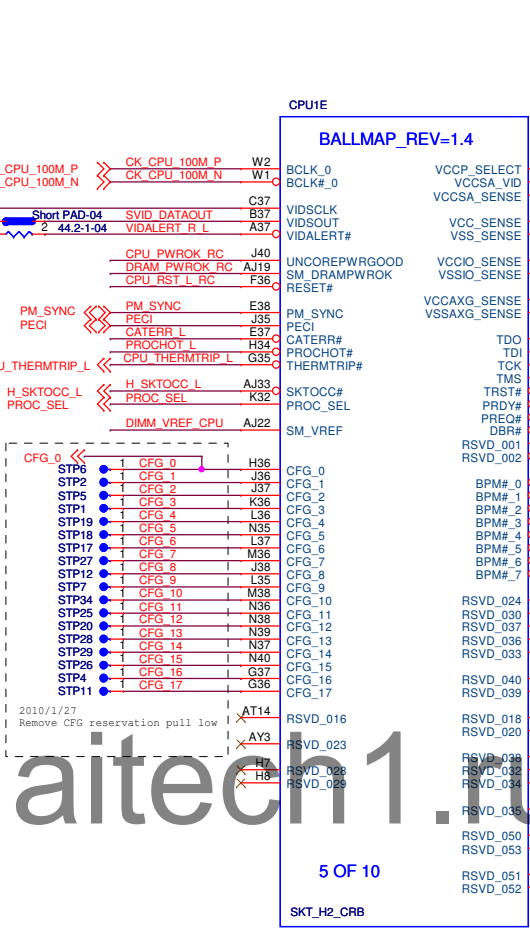
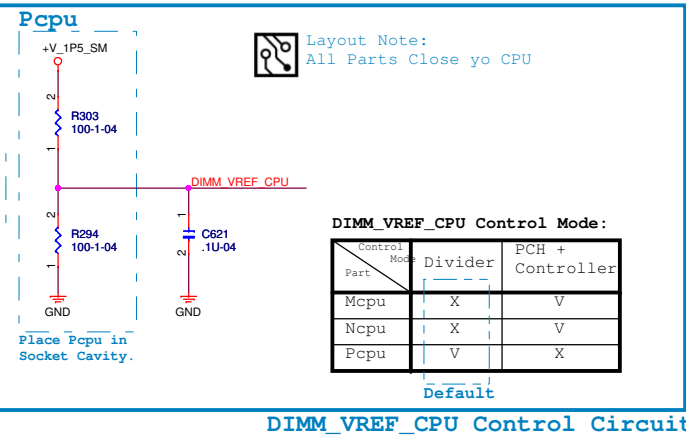
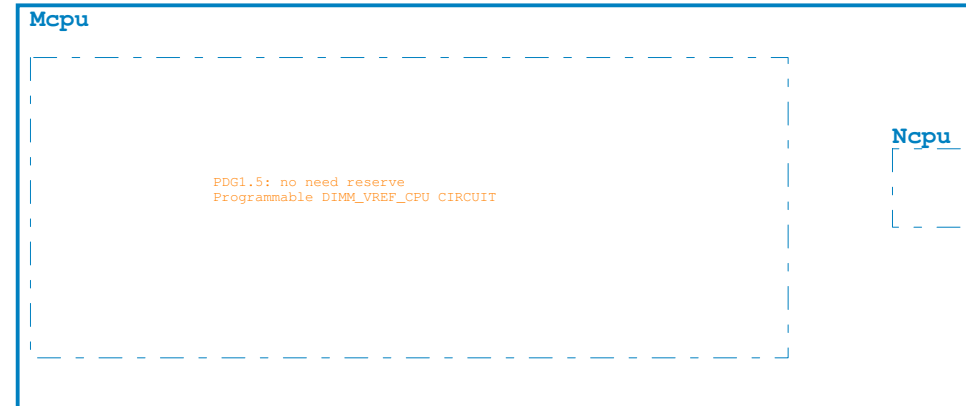
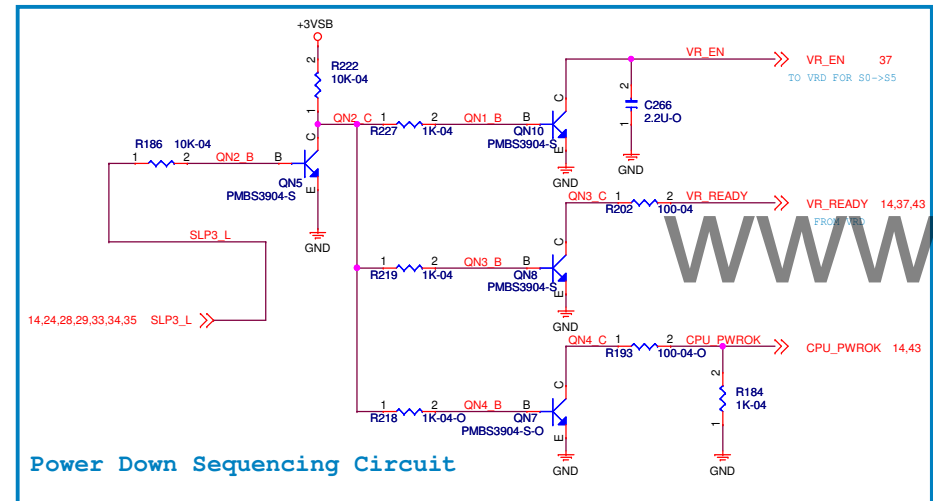
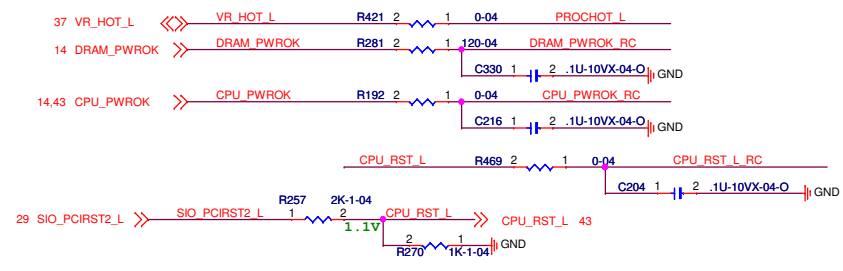
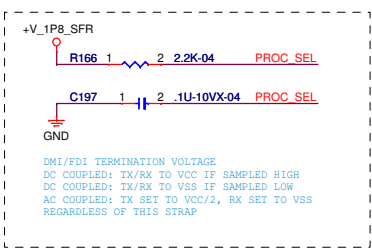


Function	INT port	PCI-E X1 port	Chipset
LAN Ethernet Controller	INTC#	PCI Express #3 Pin	Realtek RTL811E
SATA Controller	INTB#	N/A	H61 Intergrated
PCI-E to PCI Bridge	INTD#	PCI Express #4 Pin	H61 Intergrated
PCIEX1 NO.2	INTA#	PCI Express #5 Pin	H61 Intergrated
PCIEX1 NO.1	INTB#	PCI Express #6 Pin	H61 Intergrated

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GPIO & colay IVY Bridge map

Size Custom	Document Number	H61H2-AM3	Rev A
Date:	Thursday, March 01, 2012	Sheet	3 of 43



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOPGSEL[0]
6	*	*	PEOPGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

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Title: **CPU - MISC**

Size Custom: Document Number: **H61H2-AM3** Rev: **A**

Date: Thursday, March 01, 2012 Sheet: 5 of 43

9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..1]	← M_CS A L[0..1]
9 M_CKE_A[0..1]	← M_CKE A[0..1]
9 M_ODT_A[0..1]	← M_ODT A[0..1]
9 M_CLK_A_P[0..1]	← M_CLK A P[0..1]
9 M_CLK_A_N[0..1]	← M_CLK A N[0..1]
9 M_WE_A_L	← M_WE A L
9 M_CAS_A_L	← M_CAS A L
9 M_RAS_A_L	← M_RAS A L

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..1]	← M_CS B L[0..1]
10 M_CKE_B[0..1]	← M_CKE B[0..1]
10 M_ODT_B[0..1]	← M_ODT B[0..1]
10 M_CLK_B_P[0..1]	← M_CLK B P[0..1]
10 M_CLK_B_N[0..1]	← M_CLK B N[0..1]
10 M_WE_B_L	← M_WE B L
10 M_CAS_B_L	← M_CAS B L
10 M_RAS_B_L	← M_RAS B L

DDR3 CH.B

M_DATA A0	AJ3	SA_DQ_0
M_DATA A1	AJ4	SA_DQ_1
M_DATA A2	AL3	SA_DQ_2
M_DATA A3	AL4	SA_DQ_3
M_DATA A4	AJ2	SA_DQ_4
M_DATA A5	AJ1	SA_DQ_5
M_DATA A6	AL2	SA_DQ_6
M_DATA A7	AL1	SA_DQ_7
M_DATA A8	AN1	SA_DQ_8
M_DATA A9	AN4	SA_DQ_9
M_DATA A10	AR3	SA_DQ_10
M_DATA A11	AR4	SA_DQ_11
M_DATA A12	AN2	SA_DQ_12
M_DATA A13	AN3	SA_DQ_13
M_DATA A14	AR2	SA_DQ_14
M_DATA A15	AR1	SA_DQ_15
M_DATA A16	AV2	SA_DQ_16
M_DATA A17	AV3	SA_DQ_17
M_DATA A18	AV5	SA_DQ_18
M_DATA A19	AW5	SA_DQ_19
M_DATA A20	AU2	SA_DQ_20
M_DATA A21	AU3	SA_DQ_21
M_DATA A22	AU5	SA_DQ_22
M_DATA A23	AV6	SA_DQ_23
M_DATA A24	AY7	SA_DQ_24
M_DATA A25	AU7	SA_DQ_25
M_DATA A26	AV9	SA_DQ_26
M_DATA A27	AU9	SA_DQ_27
M_DATA A28	AV7	SA_DQ_28
M_DATA A29	AW7	SA_DQ_29
M_DATA A30	AW9	SA_DQ_30
M_DATA A31	AY9	SA_DQ_31
M_DATA A32	AU35	SA_DQ_32
M_DATA A33	AW37	SA_DQ_33
M_DATA A34	AU39	SA_DQ_34
M_DATA A35	AU36	SA_DQ_35
M_DATA A36	AW35	SA_DQ_36
M_DATA A37	AY36	SA_DQ_37
M_DATA A38	AU38	SA_DQ_38
M_DATA A39	AU37	SA_DQ_39
M_DATA A40	AR40	SA_DQ_40
M_DATA A41	AR37	SA_DQ_41
M_DATA A42	AN38	SA_DQ_42
M_DATA A43	AN37	SA_DQ_43
M_DATA A44	AR39	SA_DQ_44
M_DATA A45	AR38	SA_DQ_45
M_DATA A46	AN39	SA_DQ_46
M_DATA A47	AN40	SA_DQ_47
M_DATA A48	AL40	SA_DQ_48
M_DATA A49	AL37	SA_DQ_49
M_DATA A50	AJ38	SA_DQ_50
M_DATA A51	AJ37	SA_DQ_51
M_DATA A52	AL38	SA_DQ_52
M_DATA A53	AL35	SA_DQ_53
M_DATA A54	AJ40	SA_DQ_54
M_DATA A55	AG40	SA_DQ_55
M_DATA A56	AG37	SA_DQ_56
M_DATA A57	AE37	SA_DQ_57
M_DATA A58	AE38	SA_DQ_58
M_DATA A59	AE39	SA_DQ_59
M_DATA A60	AG39	SA_DQ_60
M_DATA A61	AG38	SA_DQ_61
M_DATA A62	AE39	SA_DQ_62
M_DATA A63	AE40	SA_DQ_63

M_DQS A P0	AK3	SA_DQS_0
M_DQS A P1	AP3	SA_DQS_1
M_DQS A P2	AW4	SA_DQS_2
M_DQS A P3	AV8	SA_DQS_3
M_DQS A P4	AV37	SA_DQS_4
M_DQS A P5	AP38	SA_DQS_5
M_DQS A P6	AK38	SA_DQS_6
M_DQS A P7	AF38	SA_DQS_7

M_DQS A N0	AK2	SA_DQS#_0
M_DQS A N1	AP2	SA_DQS#_1
M_DQS A N2	AV4	SA_DQS#_2
M_DQS A N3	AW8	SA_DQS#_3
M_DQS A N4	AV36	SA_DQS#_4
M_DQS A N5	AP39	SA_DQS#_5
M_DQS A N6	AK39	SA_DQS#_6
M_DQS A N7	AF39	SA_DQS#_7

SA_MA_0	AV27	M_MA A0
SA_MA_1	AV24	M_MA A1
SA_MA_2	AW24	M_MA A2
SA_MA_3	AW23	M_MA A3
SA_MA_4	AV23	M_MA A4
SA_MA_5	AT24	M_MA A5
SA_MA_6	AV24	M_MA A6
SA_MA_7	AV22	M_MA A7
SA_MA_8	AT22	M_MA A8
SA_MA_9	AV28	M_MA A9
SA_MA_10	AT21	M_MA A10
SA_MA_11	AT21	M_MA A11
SA_MA_12	AW32	M_MA A12
SA_MA_13	AU20	M_MA A13
SA_MA_14	AU20	M_MA A14
SA_MA_15	AT20	M_MA A15

SA_WE#	AW29	M_WE A L
SA_CAS#	AV30	M_CAS A L
SA_RAS#	AW28	M_RAS A L

SA_BS_0	AV29	M_BS A0
SA_BS_1	AV20	M_BS A2

SA_CS#_0	AV29	M_CS A L0
SA_CS#_1	AV32	M_CS A L1
SA_CS#_2	AW30	
SA_CS#_3	AU33	

SA_CKE_0	AV19	M_CKE A0
SA_CKE_1	AT19	M_CKE A1
SA_CKE_2	AU18	
SA_CKE_3	AV18	

SA_ODT_0	AV31	M_ODT A0
SA_ODT_1	AU32	M_ODT A1
SA_ODT_2	AU30	
SA_ODT_3	AW33	

SA_CK_0	AY25	M_CLK A P0
SA_CK#_0	AW25	M_CLK A N0
SA_CK_1	AU24	M_CLK A P1
SA_CK#_1	AW25	M_CLK A N1
SA_CK_2	AY27	
SA_CK#_2	AV26	
SA_CK_3	AW26	

SM_DRAMRST#

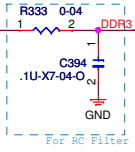
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SA_ECC_CB_4	AU15	
SA_ECC_CB_5	AU11	
SA_ECC_CB_6	AY12	
SA_ECC_CB_7	AW12	

DDR_0
3 OF 10

SKT_H2_CRB

DDR3 CH.A



desktop dosen't support ECC

Pay Attention to This Part!

M_DATA B0	AG7	SB_DQ_0
M_DATA B1	AG8	SB_DQ_1
M_DATA B2	AJ9	SB_DQ_2
M_DATA B3	AJ8	SB_DQ_3
M_DATA B4	AG5	SB_DQ_4
M_DATA B5	AG6	SB_DQ_5
M_DATA B6	AJ6	SB_DQ_6
M_DATA B7	AJ7	SB_DQ_7
M_DATA B13	AL7	SB_DQ_8
M_DATA B14	AM7	SB_DQ_9
M_DATA B11	AM10	SB_DQ_10
M_DATA B15	AL10	SB_DQ_11
M_DATA B12	AL6	SB_DQ_12
M_DATA B8	AM6	SB_DQ_13
M_DATA B14	AL9	SB_DQ_14
M_DATA B10	AM9	SB_DQ_15
M_DATA B16	AP7	SB_DQ_16
M_DATA B17	AP7	SB_DQ_17
M_DATA B18	AP10	SB_DQ_18
M_DATA B19	AR10	SB_DQ_19
M_DATA B20	AP6	SB_DQ_20
M_DATA B21	AP6	SB_DQ_21
M_DATA B22	AP9	SB_DQ_22
M_DATA B23	AM12	SB_DQ_23
M_DATA B24	AM12	SB_DQ_24
M_DATA B25	AM13	SB_DQ_25
M_DATA B26	AR13	SB_DQ_26
M_DATA B27	AP13	SB_DQ_27
M_DATA B28	AL12	SB_DQ_28
M_DATA B29	AL13	SB_DQ_29
M_DATA B30	AR12	SB_DQ_30
M_DATA B31	AP12	SB_DQ_31
M_DATA B32	AR28	SB_DQ_32
M_DATA B33	AR29	SB_DQ_33
M_DATA B34	AL28	SB_DQ_34
M_DATA B35	AL29	SB_DQ_35
M_DATA B36	AP28	SB_DQ_36
M_DATA B37	AP29	SB_DQ_37
M_DATA B38	AM28	SB_DQ_38
M_DATA B39	AM29	SB_DQ_39
M_DATA B40	AP32	SB_DQ_40
M_DATA B41	AP31	SB_DQ_41
M_DATA B42	AP35	SB_DQ_42
M_DATA B43	AP34	SB_DQ_43
M_DATA B44	AR30	SB_DQ_44
M_DATA B45	AR31	SB_DQ_45
M_DATA B46	AR32	SB_DQ_46
M_DATA B47	AR34	SB_DQ_47
M_DATA B48	AM32	SB_DQ_48
M_DATA B52	AM31	SB_DQ_49
M_DATA B55	AL35	SB_DQ_50
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M_DATA B54	AM34	SB_DQ_52
M_DATA B49	AL31	SB_DQ_53
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M_DATA B57	AR34	SB_DQ_57
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M_DATA B59	AE35	SB_DQ_59
M_DATA B60	AJ35	SB_DQ_60
M_DATA B61	AJ34	SB_DQ_61
M_DATA B62	AF33	SB_DQ_62
M_DATA B63	AF35	SB_DQ_63

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M_DQS B P2	AP8	SB_DQS_2
M_DQS B P3	AN13	SB_DQS_3
M_DQS B P4	AN29	SB_DQS_4
M_DQS B P5	AP33	SB_DQS_5
M_DQS B P6	AL33	SB_DQS_6
M_DQS B P7	AG35	SB_DQS_7

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SB_MA_7	AL18	M_MA B7
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SB_MA_9	AY17	M_MA B9
SB_MA_10	AN23	M_MA B10
SB_MA_11	AU17	M_MA B11
SB_MA_12	AT18	M_MA B12
SB_MA_13	AR26	M_MA B13
SB_MA_14	AY16	M_MA B14
SB_MA_15	AV16	M_MA B15

SA_CK[2]	AR25	M_WE B L
SA_CK[1]	AK25	M_CAS B L
SA_ODT[2]	AP24	M_RAS B L

SB_BS_0	AP23	M_BS B0
SB_BS_1	AM24	M_BS B1
SB_BS_2	AW17	M_BS B2

SB_CS#_0	AN25	M_CS B L0
SB_CS#_1	AN26	M_CS B L1
SB_CS#_2	AL25	
SB_CS#_3	AT28	

SB_CKE_0	AU16	M_CKE B0
SB_CKE_1	AY15	M_CKE B1
SB_CKE_2	AW15	
SB_CKE_3	AV15	

SB_ODT_0	AL26	M_ODT B0
SB_ODT_1	AP26	M_ODT B1
SB_ODT_2	AM26	
SB_ODT_3	AK26	

SB_CK_0	AL21	M_CLK B P0
SB_CK#_0	AL22	M_CLK B N0
SB_CK_1	AL20	M_CLK B P1
SB_CK#_1	AK20	M_CLK B N1
SB_CK_2	AL23	
SB_CK#_2	AM22	
SB_CK_3	AP21	
SB_CK#_3	AN21	

SB_DRAMRST#

SB_DQS_8	AN16	
SB_DQS#_8	AN15	

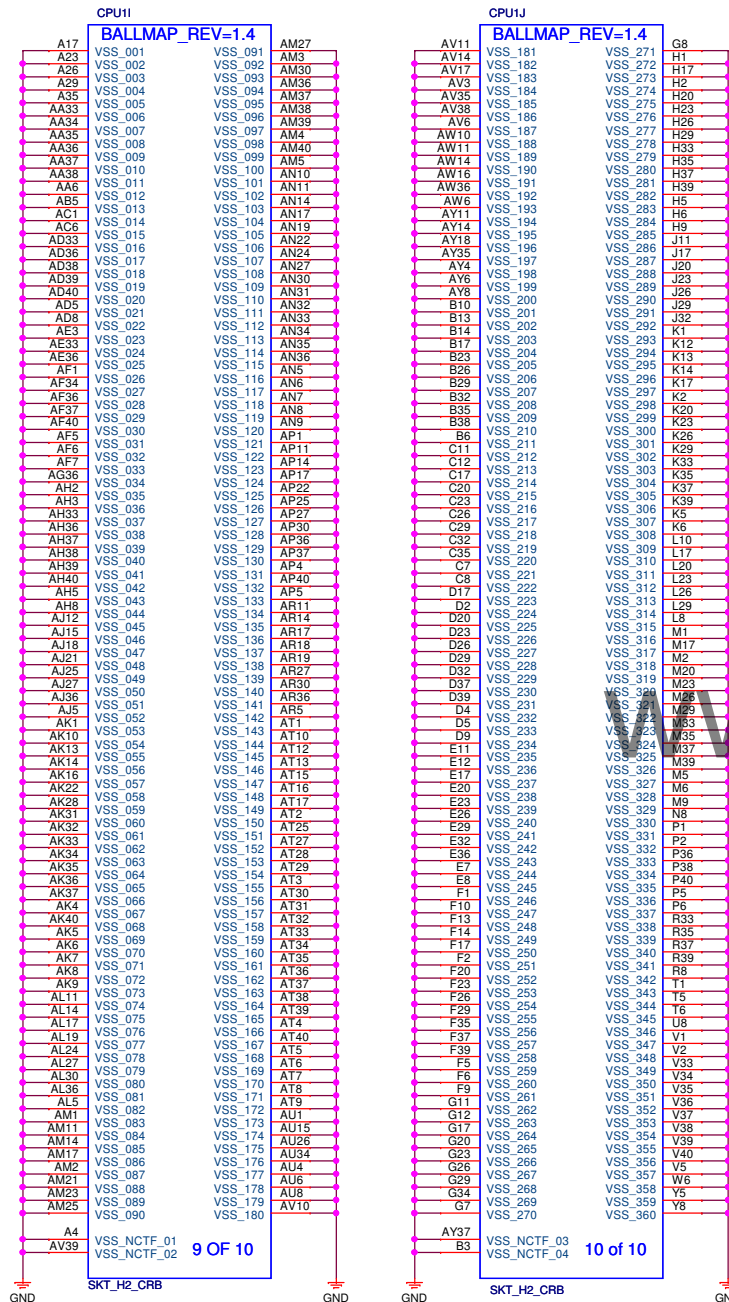
SB_ECC_CB_0	AL16	
SB_ECC_CB_1	AM16	
SB_ECC_CB_2	AP16	
SB_ECC_CB_3	AR16	
SB_ECC_CB_4	AT15	
SB_ECC_CB_5	AR15	
SB_ECC_CB_6	AT15	
SB_ECC_CB_7	AR15	

DDR_1
4 OF 10

SKT_H2_CRB

DDR3 CH.B

desktop dosen't support ECC

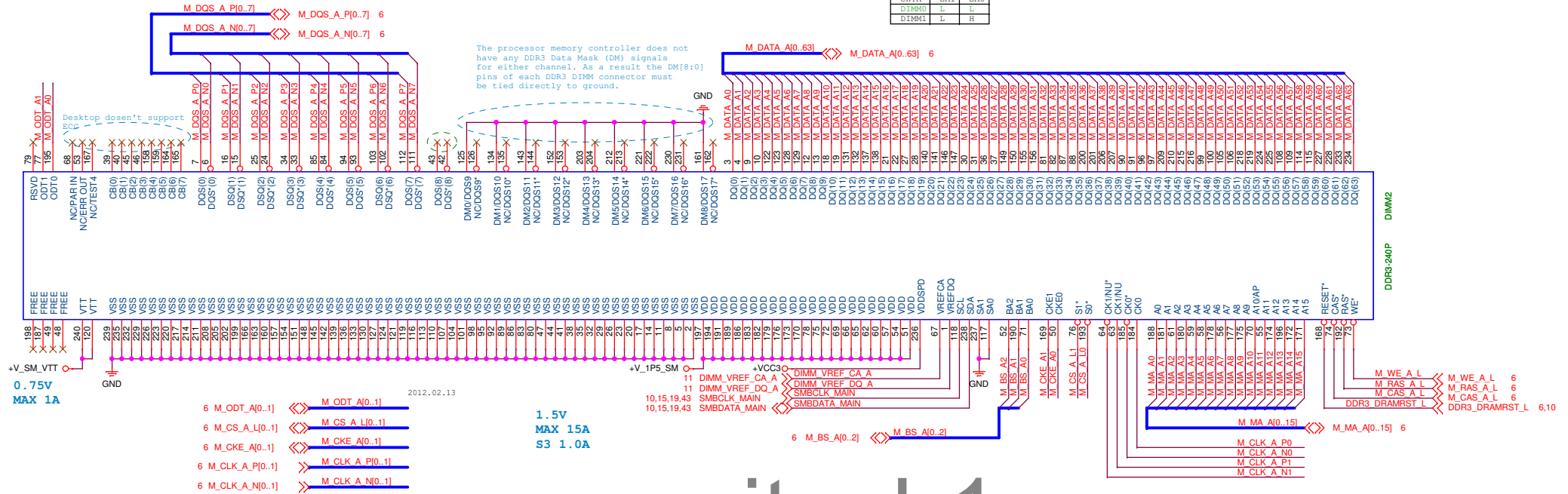


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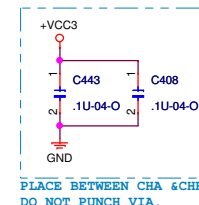
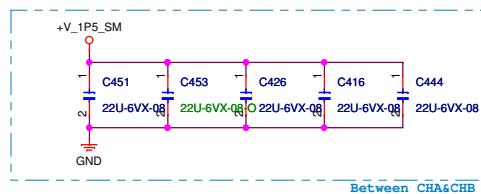
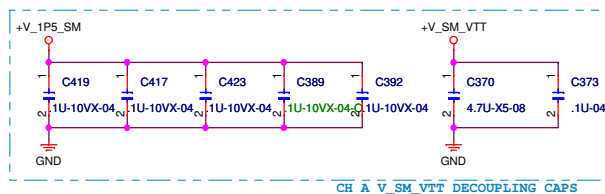
CHANNEL A DIMM

CH_A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



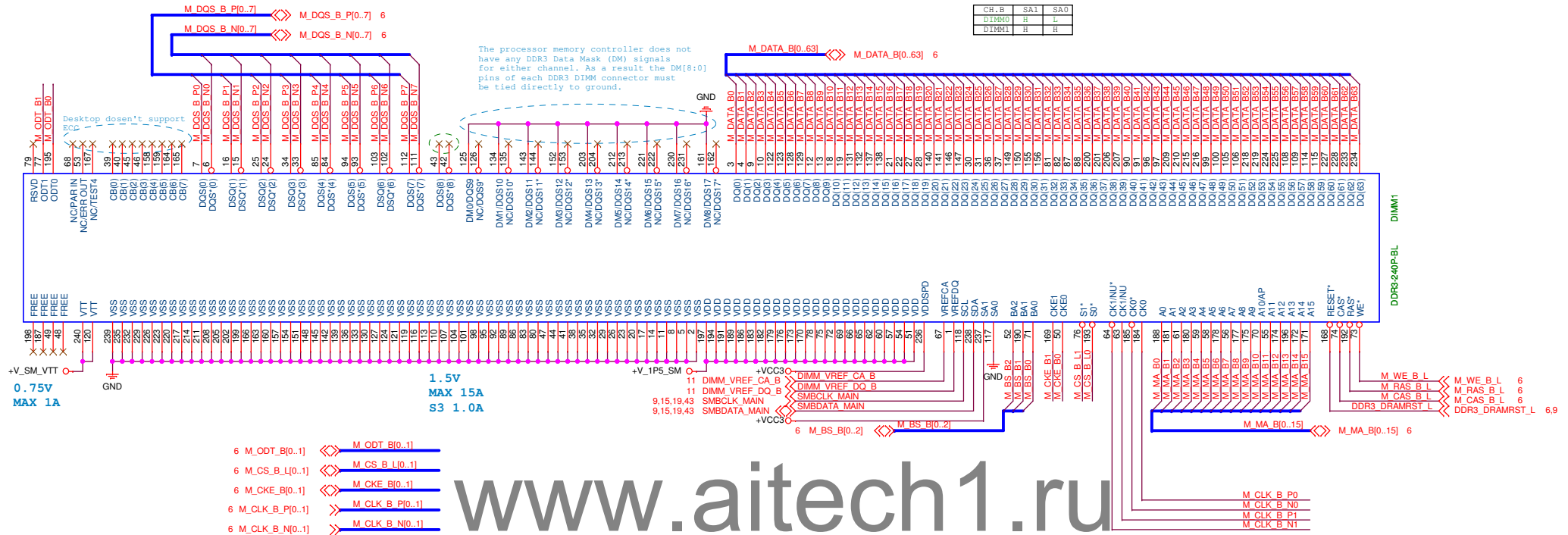
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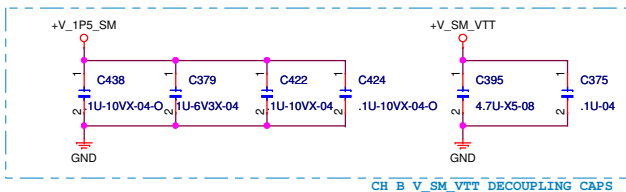
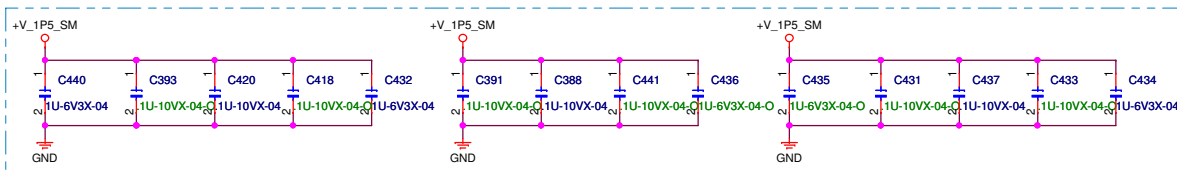
CHANNEL B DIMMs

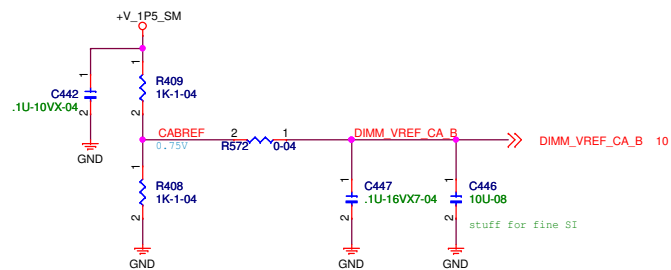
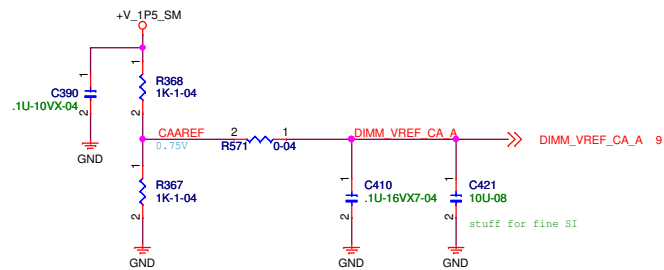
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

CH_B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

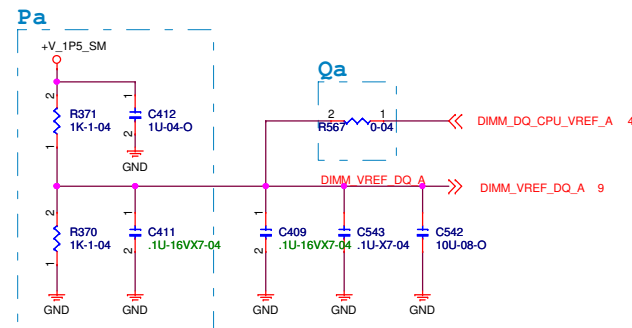


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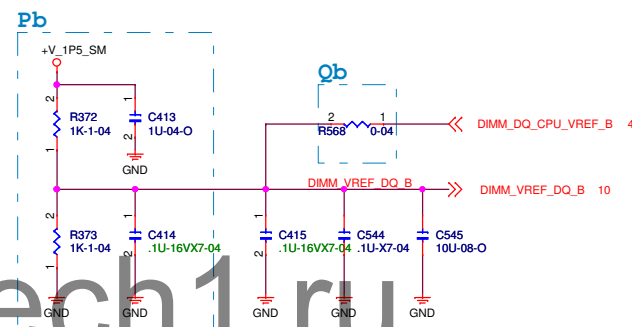




DIMM_VREF_CA Circuit



Layout Note:
All parts close to DDR3 Slots.



DIMM_VREF_DQ Control Circuit

DIMM_VREF_DQ Control Mode:

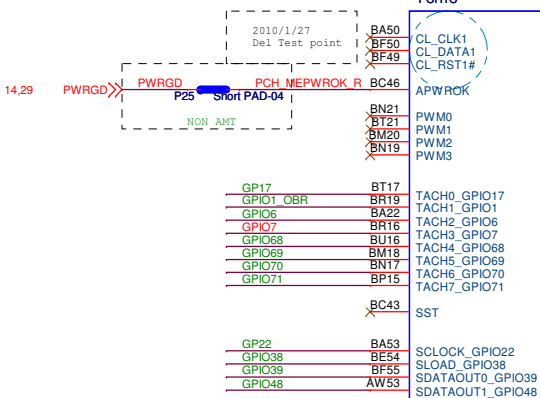
Control Part	Mode	CPU	Divider
Pz	X	V	
Qz	V	V	

Z=a,b

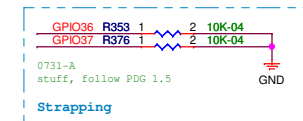
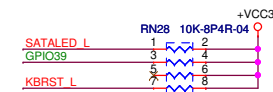
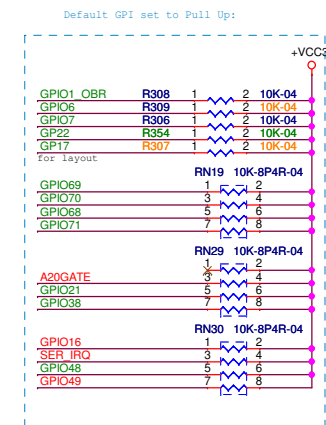
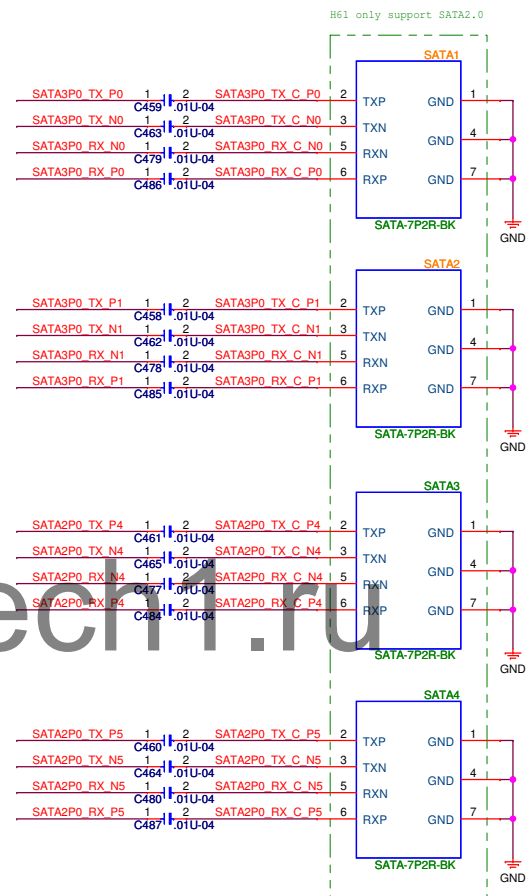
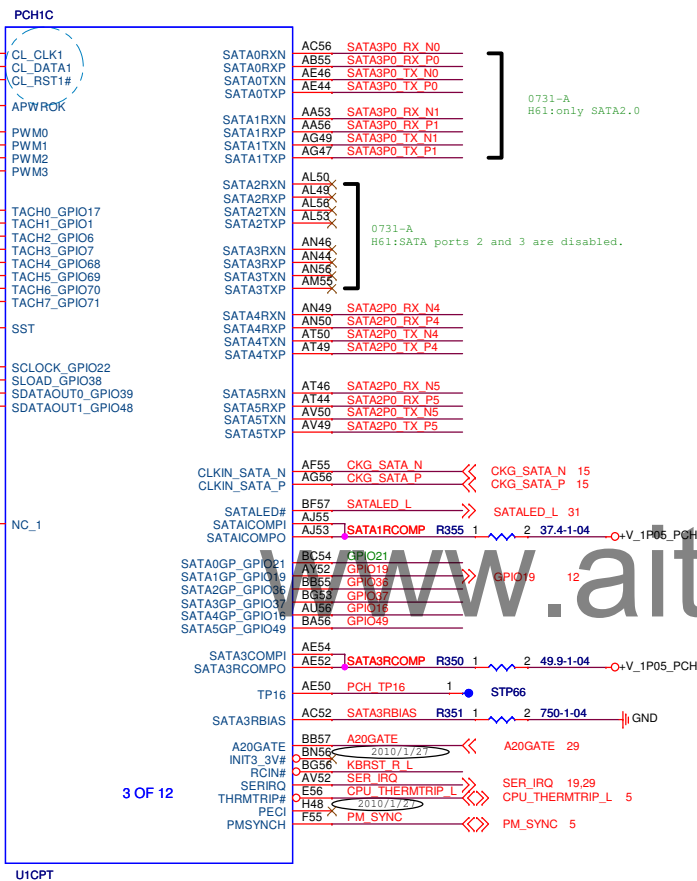
Default

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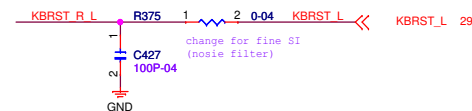
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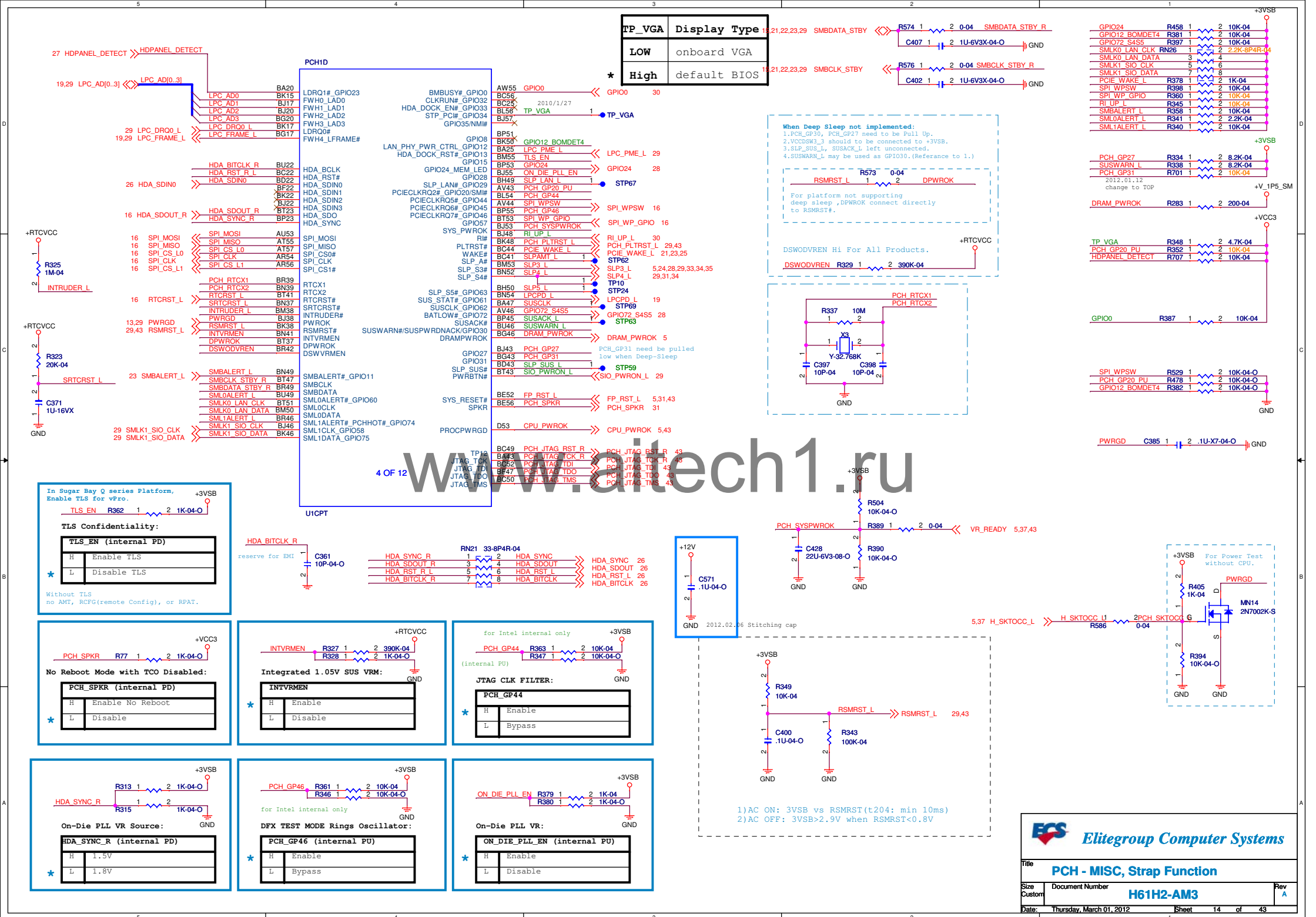


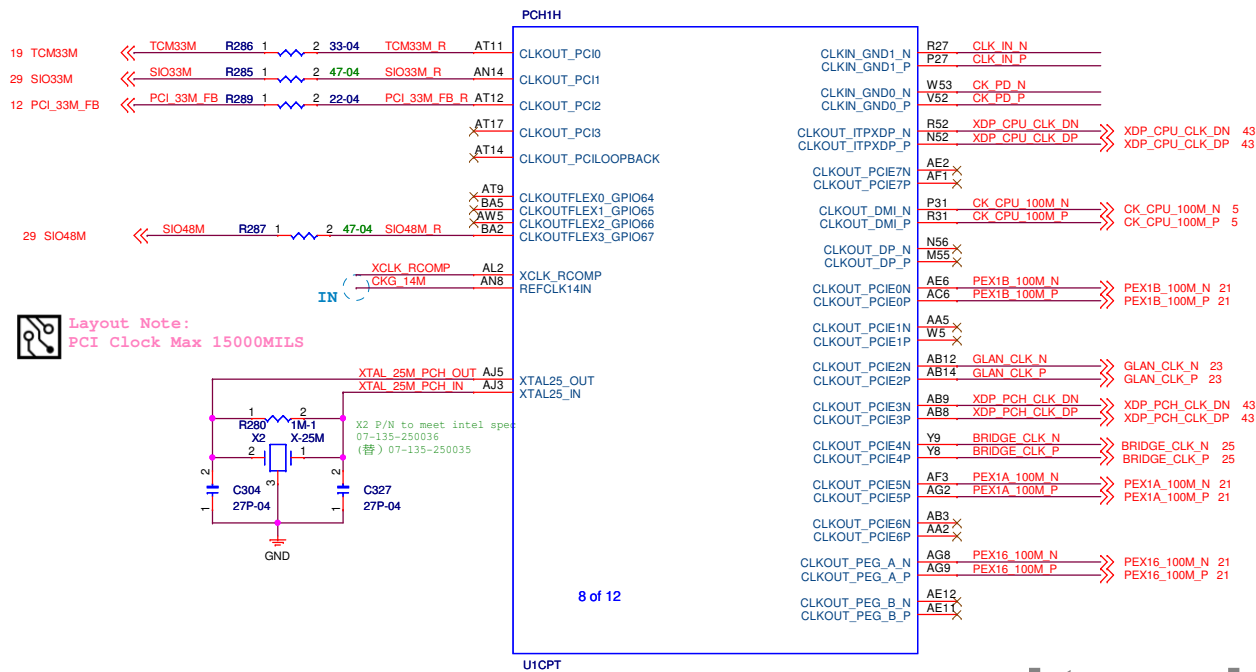
3 OF 12



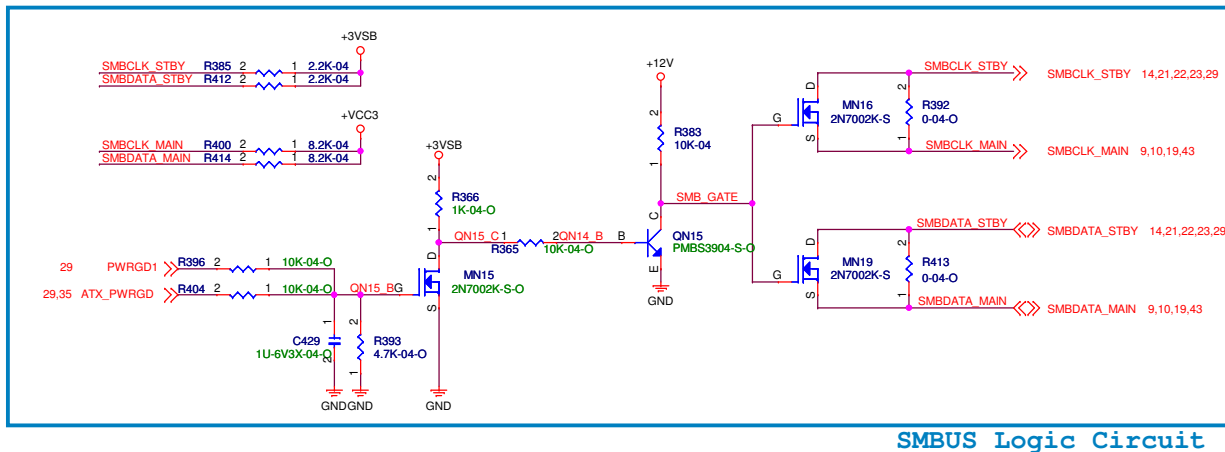
Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω
±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω
±17.5%

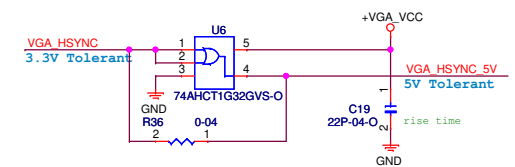
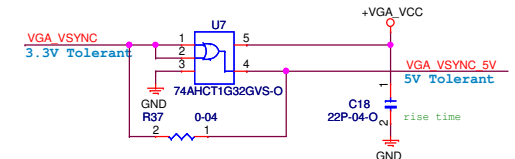
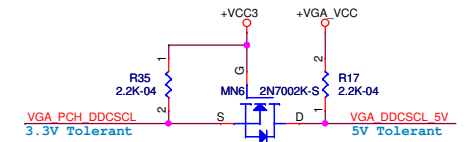
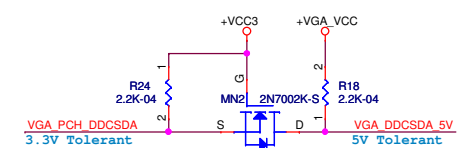
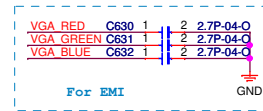
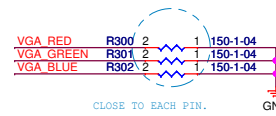
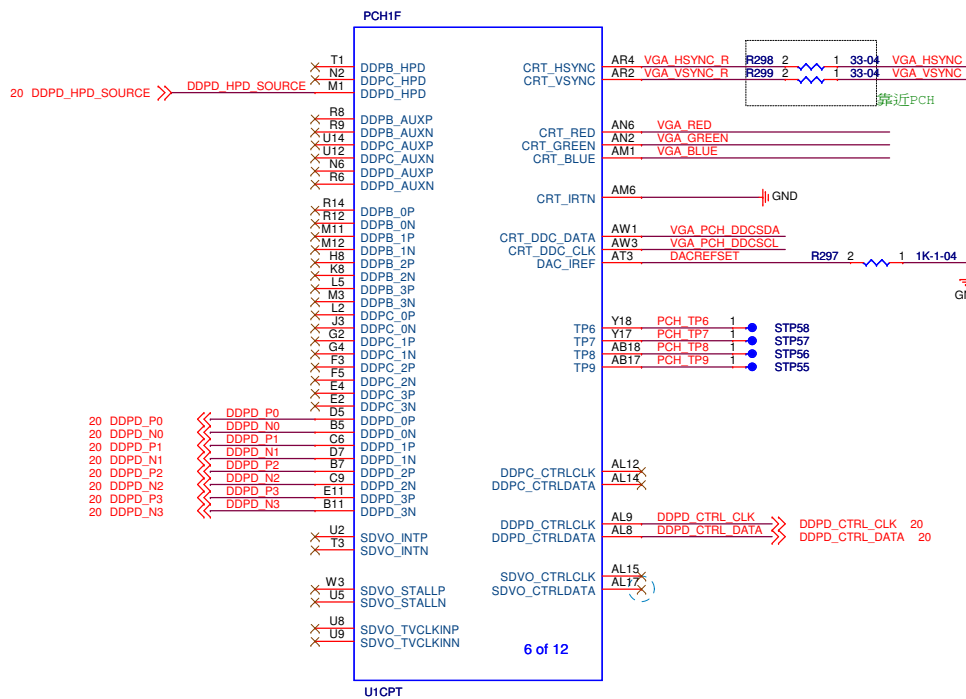




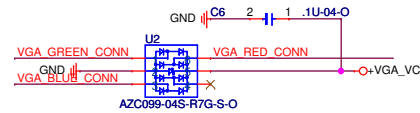
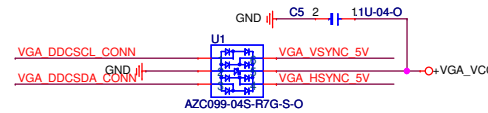
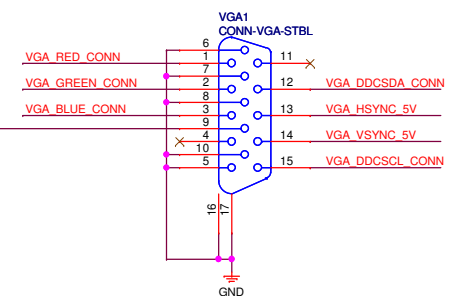
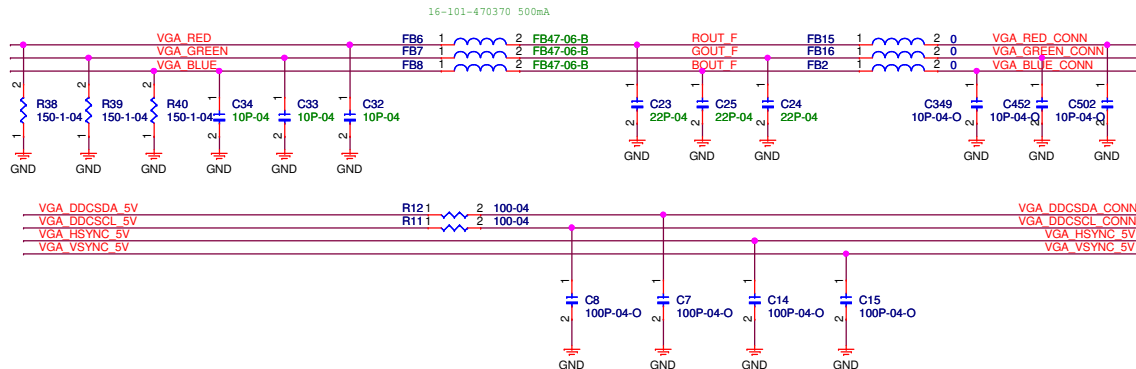
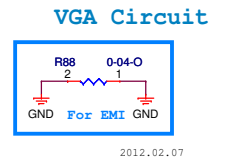
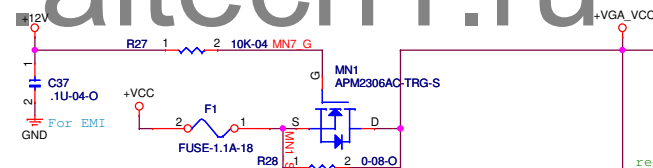


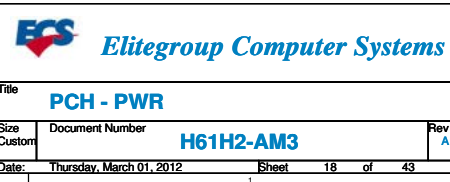
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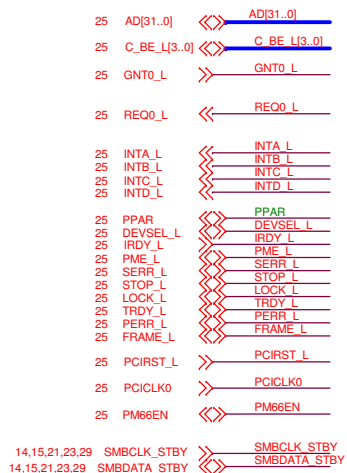


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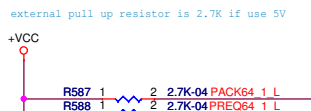
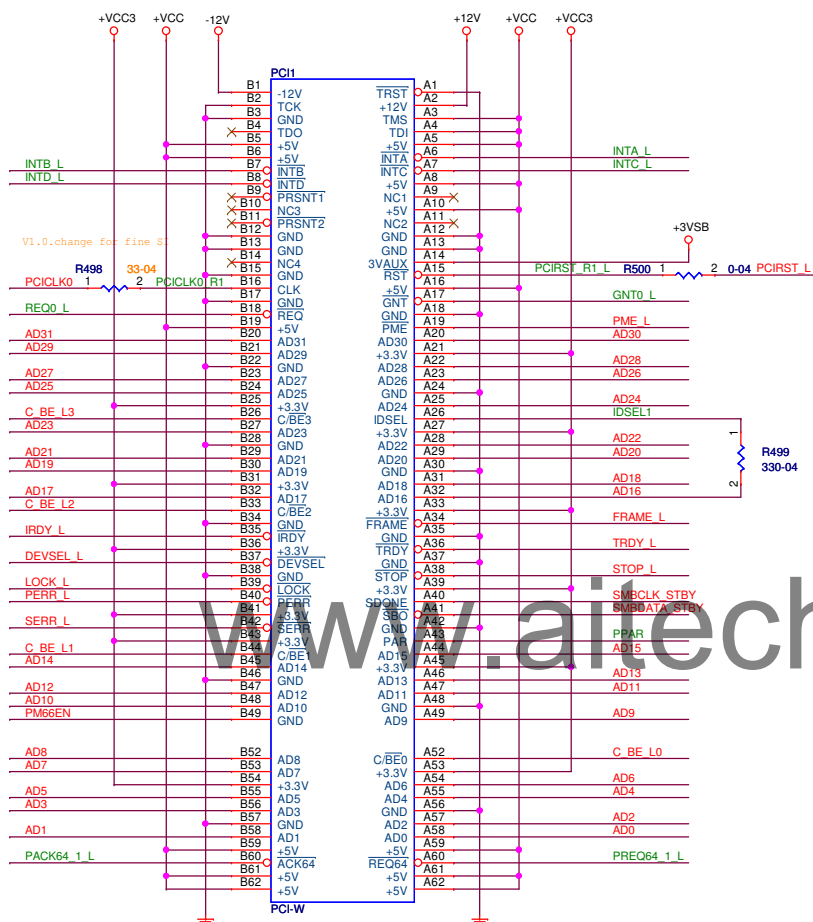




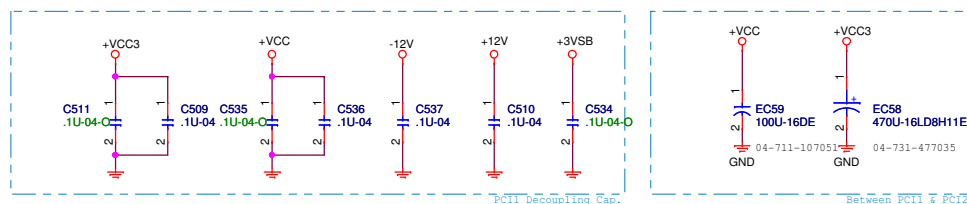
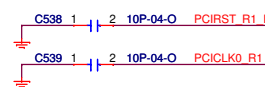
www.aitech1.ru

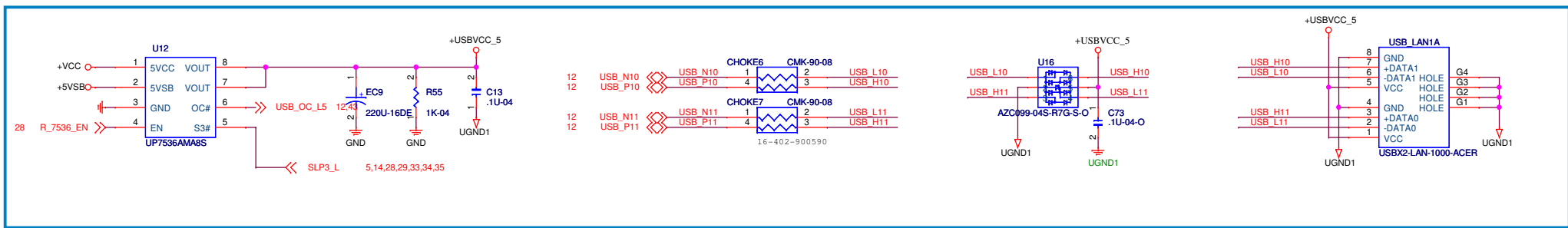


PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

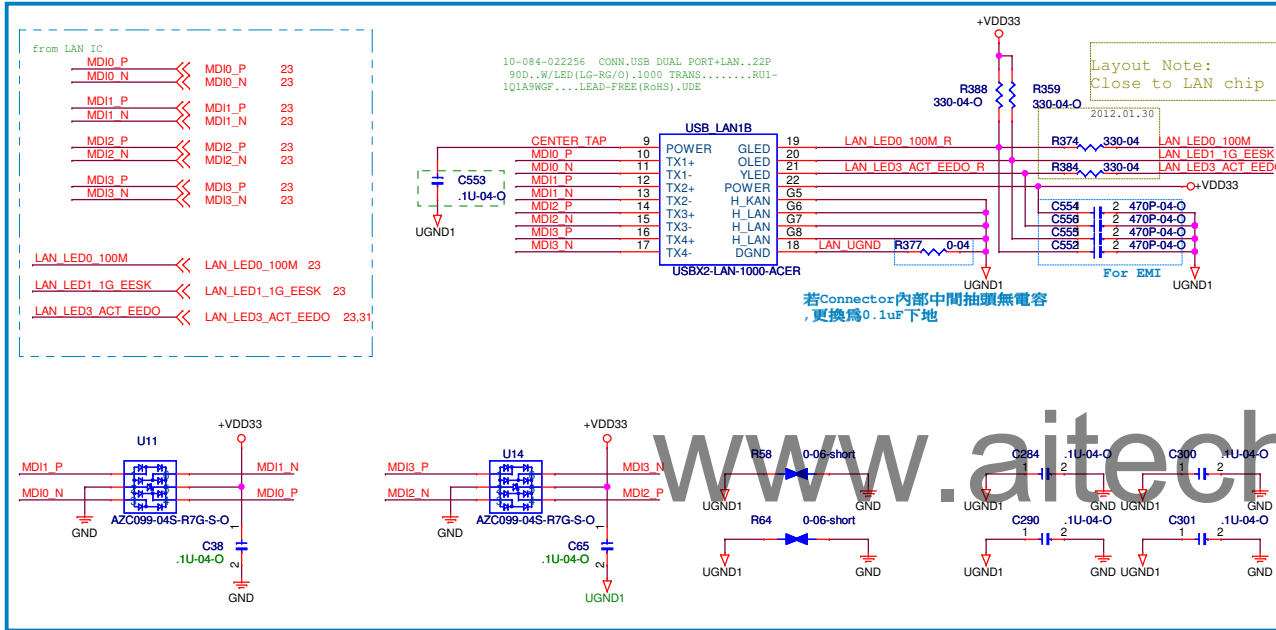


IDSEL=AD16
INT[A,B,C,D]
Legacy mode from PCH
INT[A,B,C,D]





REAR SIDE 2 PORTS ON LANUSB CONN.



REAR SIDE 2 PORTS ON LANUSB CONN.

Acer Lan LED Status

Wake on LAN (WOL) set to ON ==> In BIOS and OS								
	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access: Blink	Blink	Blink	Blink	Blink	Blink	OFF
		Others: OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected: OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000: ON with A color: Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100: ON with B color: Green	Green	OFF	OFF	OFF	OFF	OFF
		10: OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF

Wake on LAN (WOL) set to OFF ==> In BIOS and OS								
	LED	S0	S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access: Blink	Blink	OFF	OFF	OFF	OFF	OFF
		Others: OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected: OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000: ON with A color: Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100: ON with B color: Green	Green	OFF	OFF	OFF	OFF	OFF
	10: OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF	OFF

Table 12. Customized LEDs				
	LINK	LINK	LINK	ACT/Full
Speed	Link 10M	Link 100M	Link 1000M	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
Not Defined	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

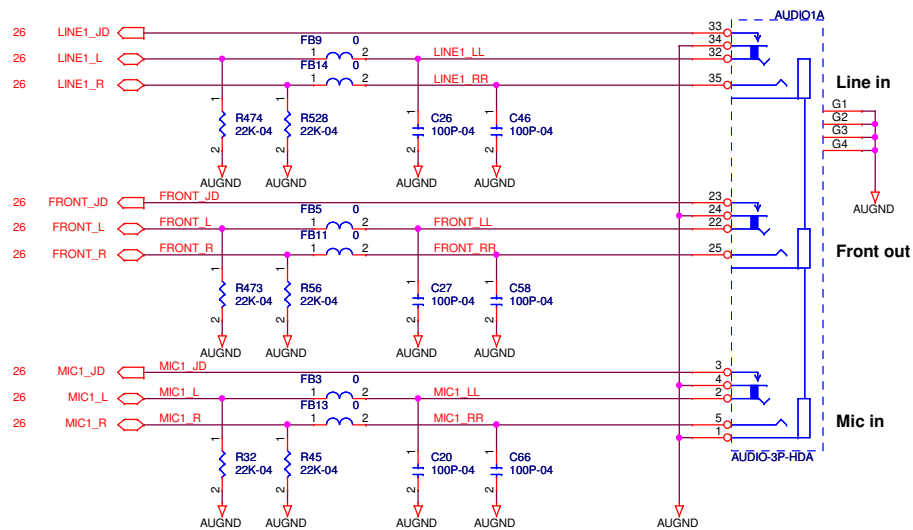
LED Pin	ACT=0	ACT=1
LINK=0	Flashing	All Speed ACT
LINK=0	Selected Speed LINK	Selected Speed LINK=ACT

Note1: ACT means blinking TX and RX LINK indicates Link 10M/100M/1000M.
Note2: There are four special modes:
Mode A: LED OFF Mode → Set all bits to 0
Mode B: Full Duplex LED Mode → Set LED 0=0, and either LED 1 or LED 3 = 0
Mode C: Separated TX/RX Mode → LED 0=TX, LED 1=RX, LED 3=LINK
Mode D: Separated Speed ACT Mode → Set LED 0=0, LED 1=1, LED 3=1
LED 0=10ACT
LED 1=100ACT
LED 3=1000ACT

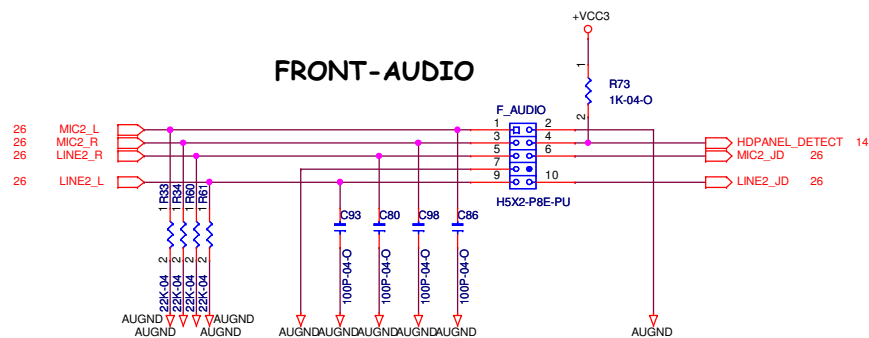
Acer Spec:

LAN LED	
Active	Green
LINK1000	Orange
LINK100	Green
LINK10	OFF

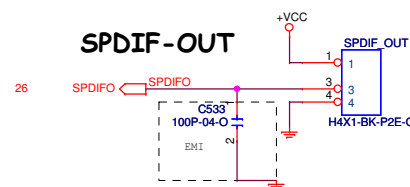
REAR-AUDIO



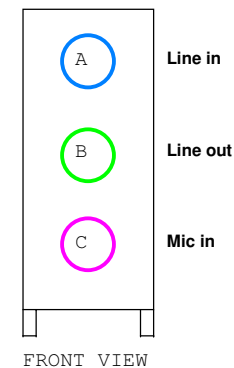
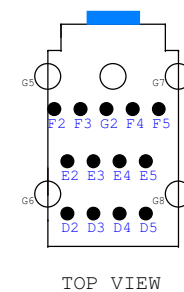
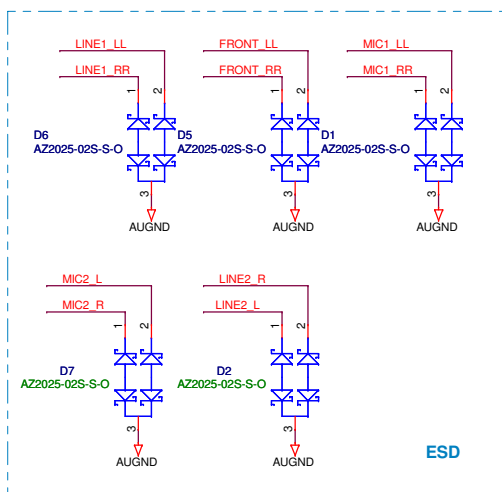
FRONT-AUDIO



SPDIF-OUT



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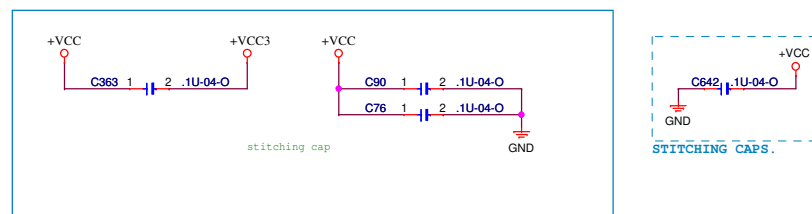
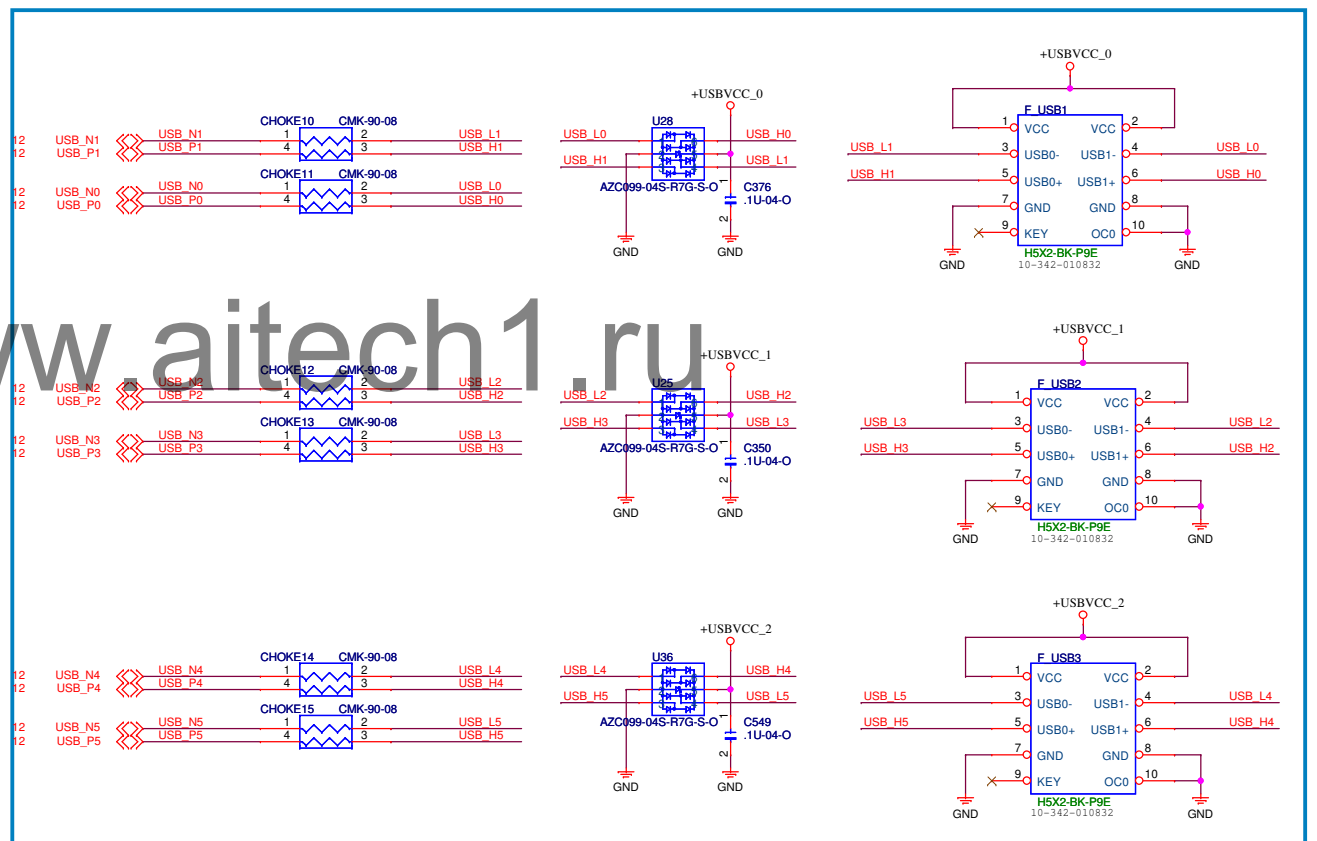
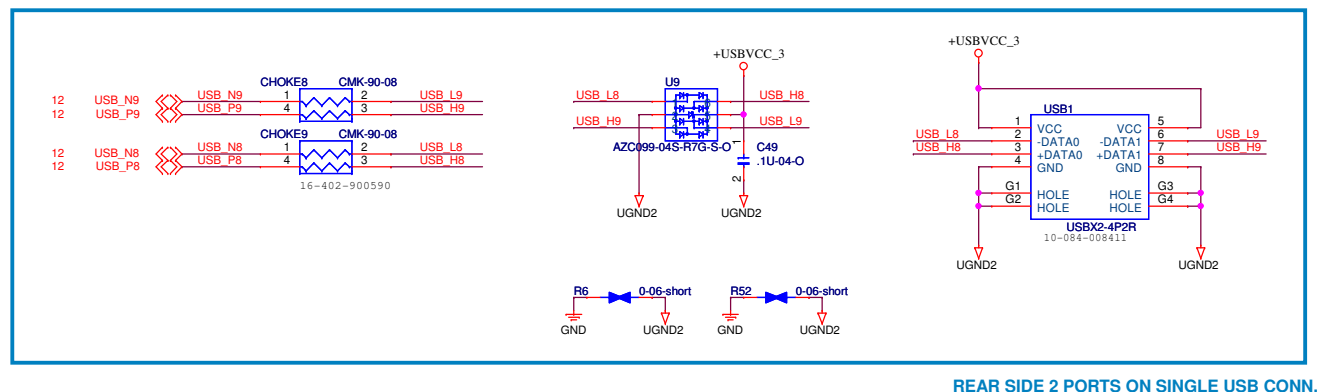
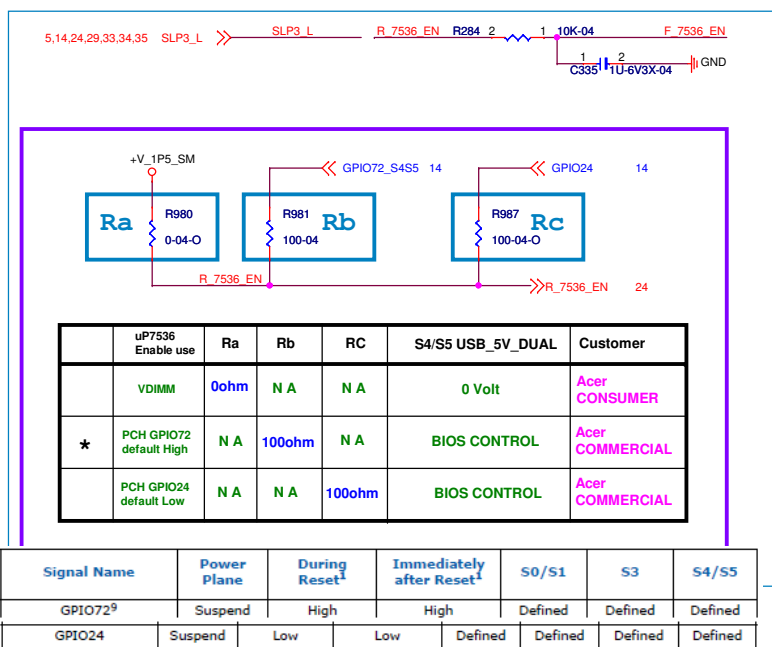
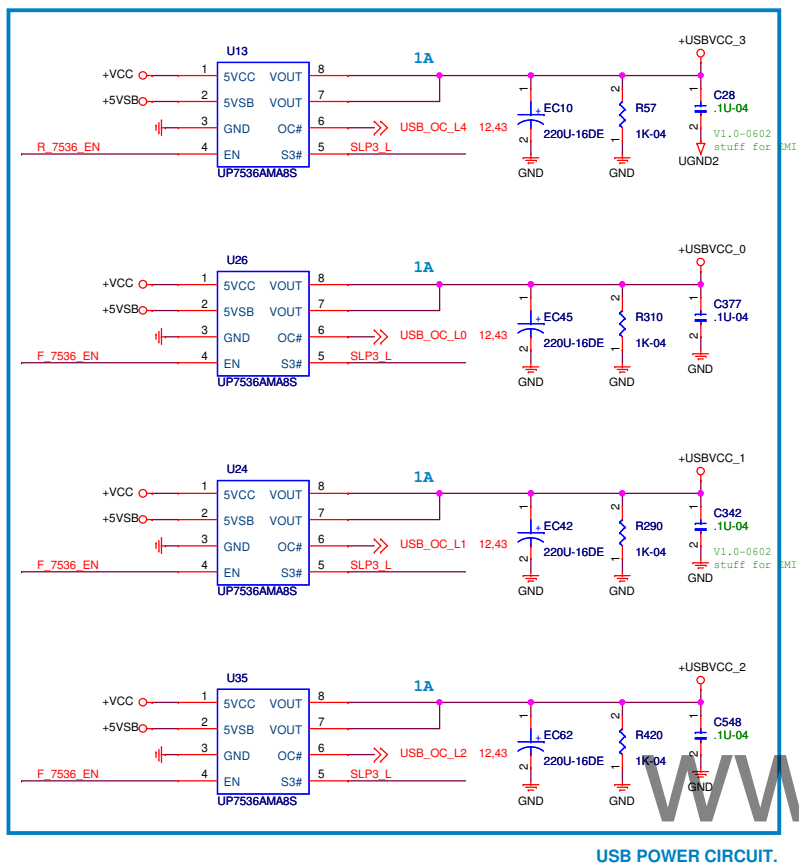


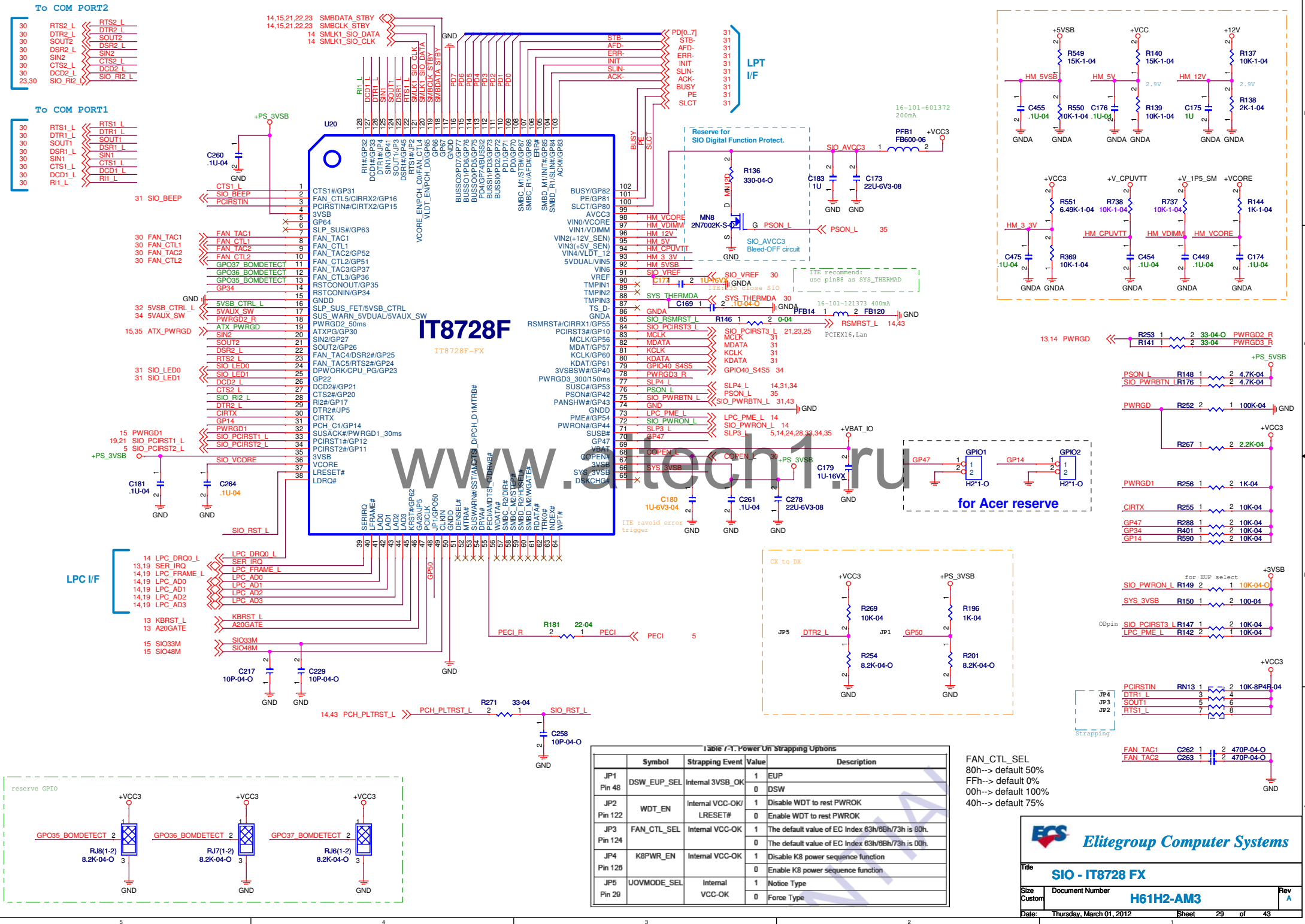
ECS Elitegroup Computer Systems

Title: **Audio - CONN/HDR**


Size: Custom Document Number: **H61H2-AM3** Rev: A

Date: Thursday, March 01, 2012 Sheet: 27 of 43





FAN_CTL_SEL
80h--> default 50%
FFh--> default 0%
00h--> default 100%
40h--> default 75%



Elitegroup Computer Systems

Title

SIO - IT8728 FX

Size

Document Number

H61H2-AM3

Custom

Rev

A

Date:

Thursday, March 01, 2012

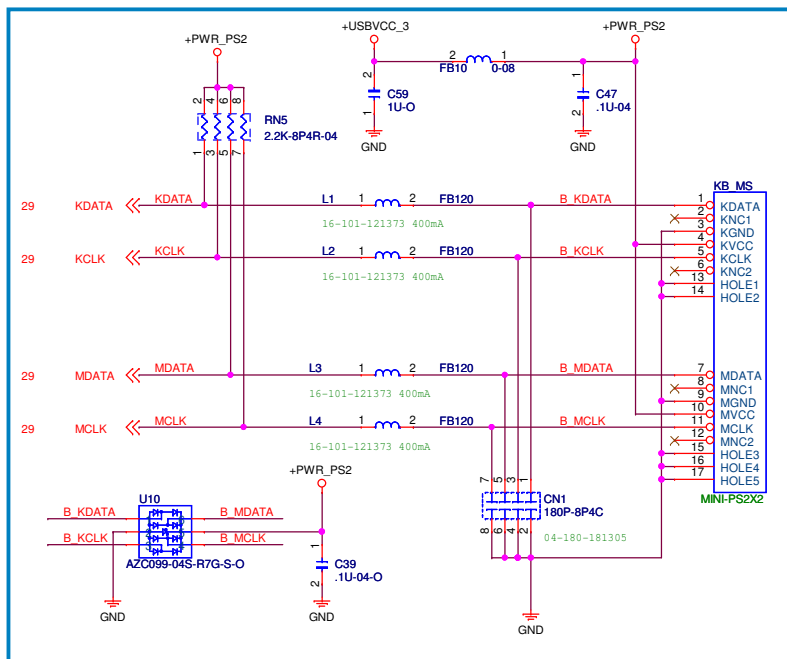
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29

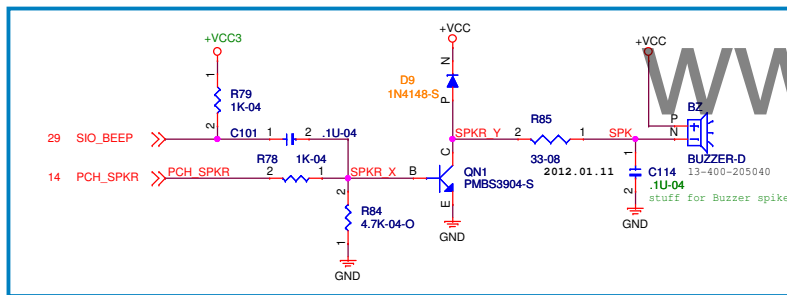
of

43

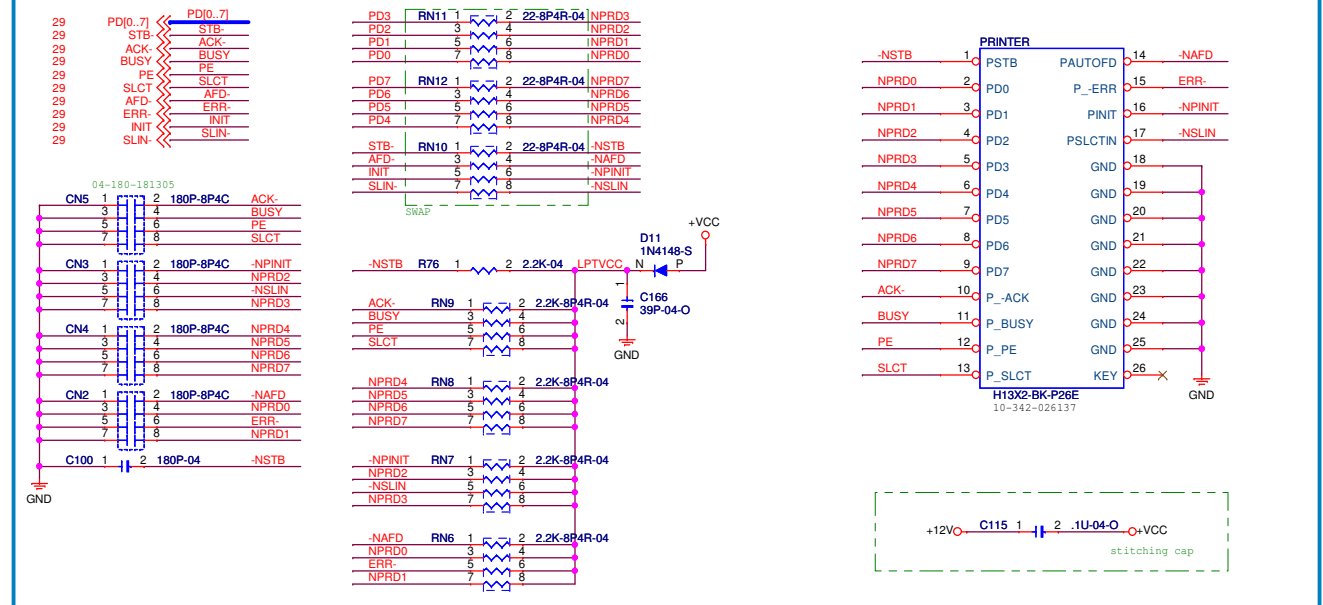
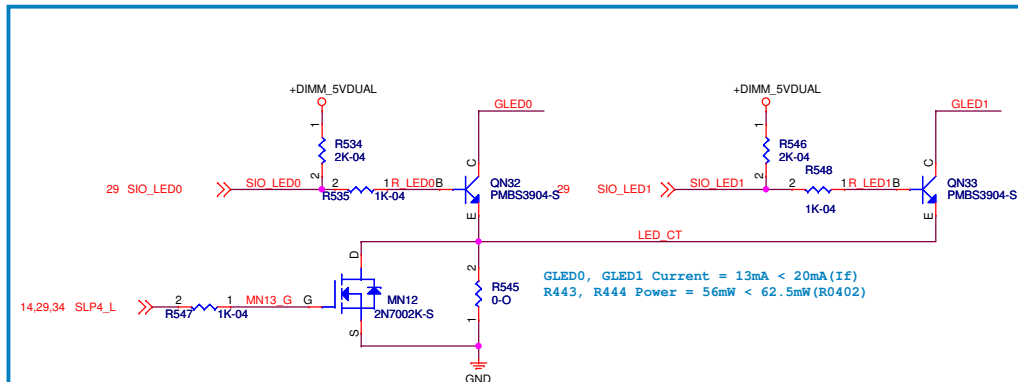
Table 1-1: Power On Strapping Options				
Symbol	Strapping Event	Value	Description	
JP1 Pin 48	DSW_EUP_SEL	Internal 3VSB_OK	1 EUP	
			0 DSW	
JP2 Pin 122	WDT_EN	Internal VCC-OK/ LRESET#	1 Disable WDT to rest PWROK	
			0 Enable WDT to rest PWROK	
JP3 Pin 124	FAN_CTL_SEL	Internal VCC-OK	1 The default value of EC Index 63h/6Bh/73h is 80h.	
			0 The default value of EC Index 63h/6Bh/73h is 00h.	
JP4 Pin 126	KBPWR_EN	Internal VCC-OK	1 Disable K8 power sequence function	
			0 Enable K8 power sequence function	
JP5 Pin 29	UOVMODE_SEL	Internal VCC-OK	1 Notice Type	
			0 Force Type	



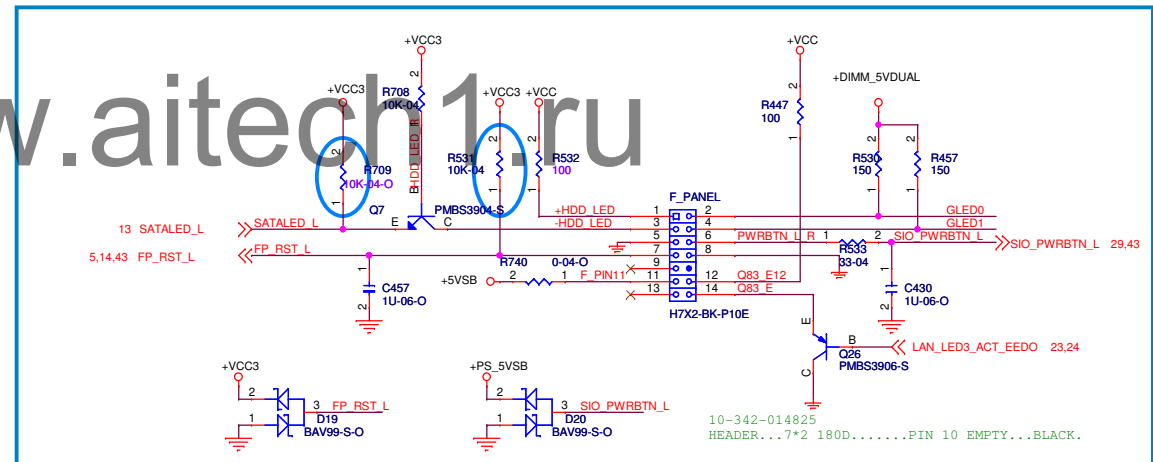
PS2 Circuit



Buzzer Circuit



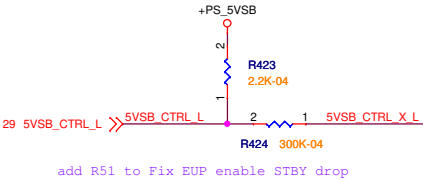
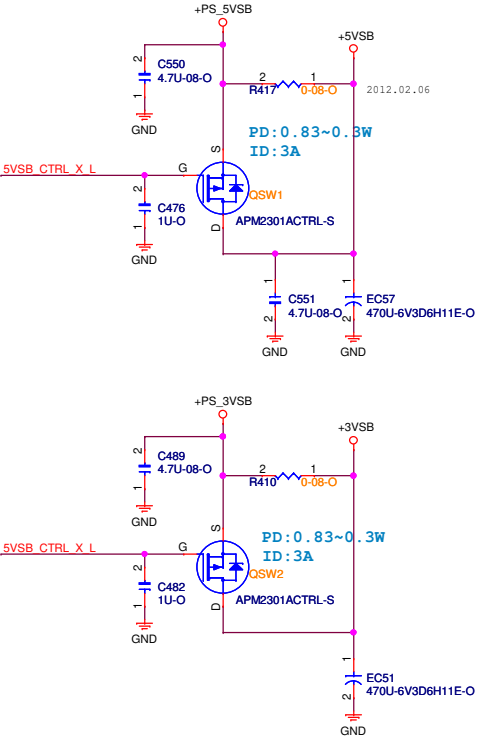
LPT Header Circuit



Front Panel Circuit

	LED	S0	S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF

EuP Lot6 Power Saving Circuit



Layout Note:
Close to ATX 24P2R Connector.

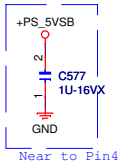
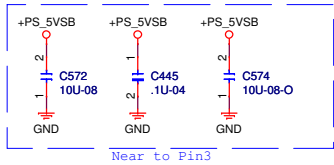
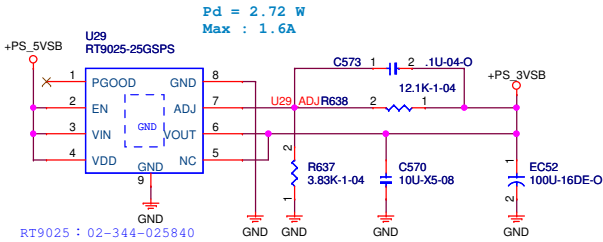
EuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF

* China one Enery Saving Spec

Customer	S3	S5
TP	< 0.4A	< 0.18A
FDR	< 0.8A	< 0.15A

+3VSB Circuit



3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
TPM(WPCT210)	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

5	4	3	2	1
---	---	---	---	---



C

V1P8_SFR (1.5A max)



del 1.05V ME power

V1P05_ME

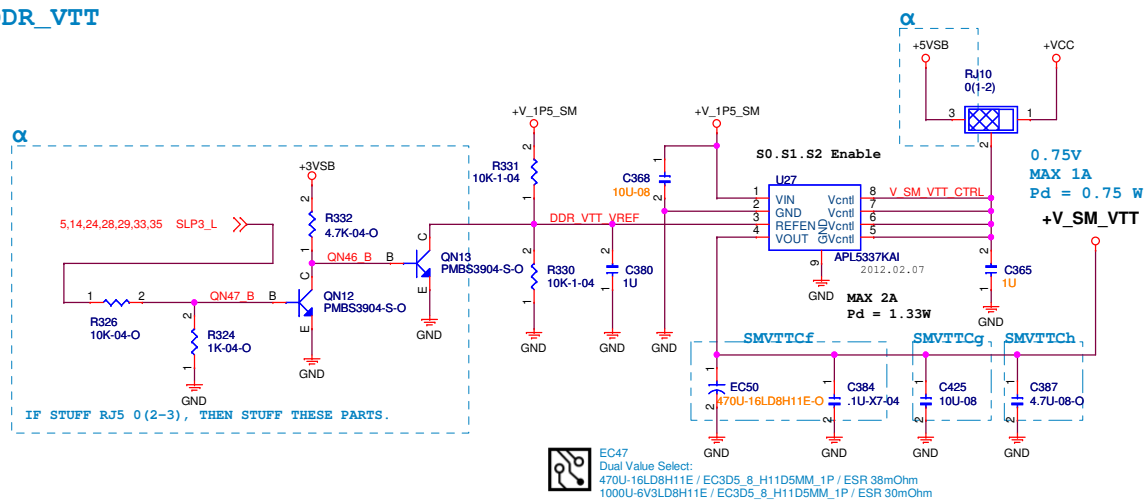
V1P05_ME

RT8120FGS
IC PWM.RT8120FGS..SOP 8P.0.8
V....HF.LEAD-FREE.RICHTEK

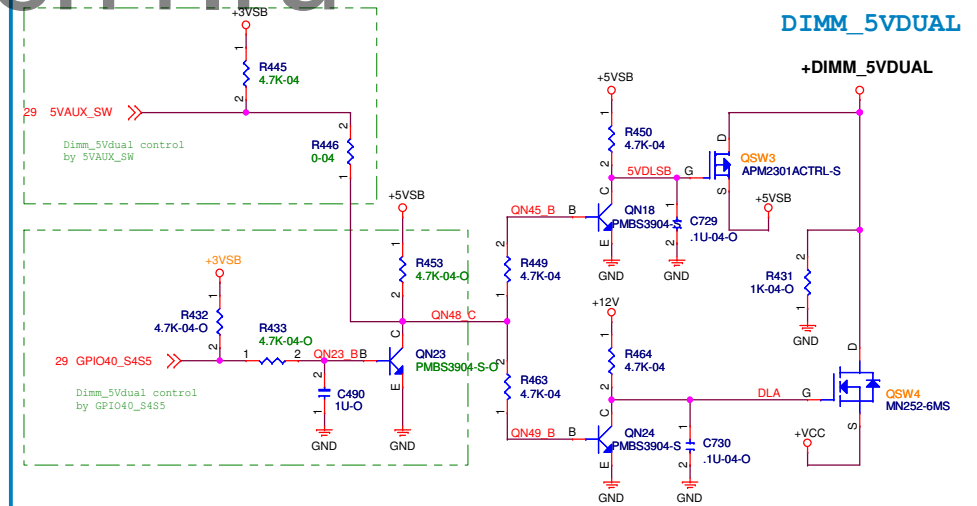


VDDQ= $0.8 \cdot (1 + R466/R467)$

α



 EC47
Dual Value Select:
470U-16LD8H11E / EC3D5_8_H11D5MM_1P / ESR 38mOhm
1000U-6V3LD8H11E / EC3D5_8_H11D5MM_1P / ESR 30mOhm

*

stuff VSAGz

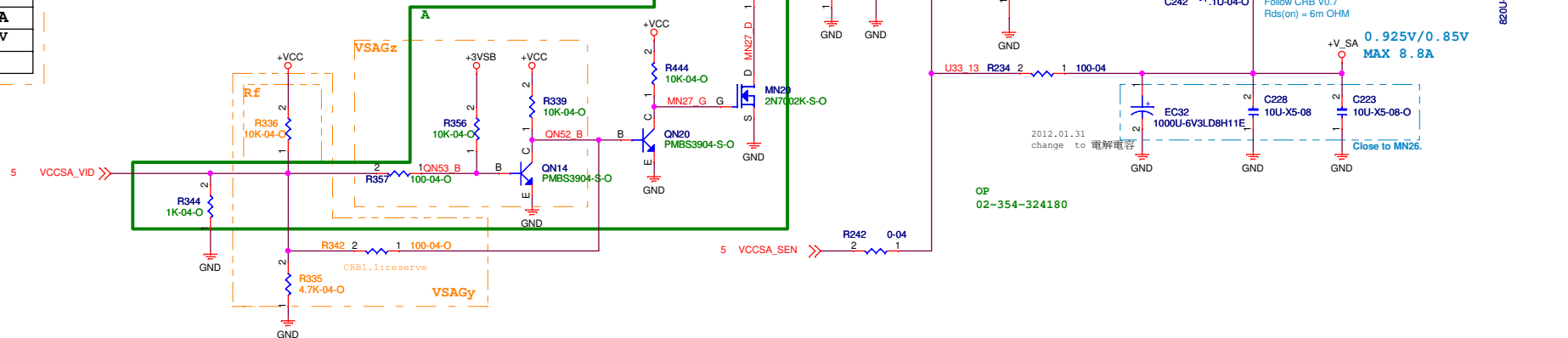
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

stuff VSAGy

VCCSA voltage selection	
Rf	+V_SA
stuff	0.925V
unstuff	0.85V

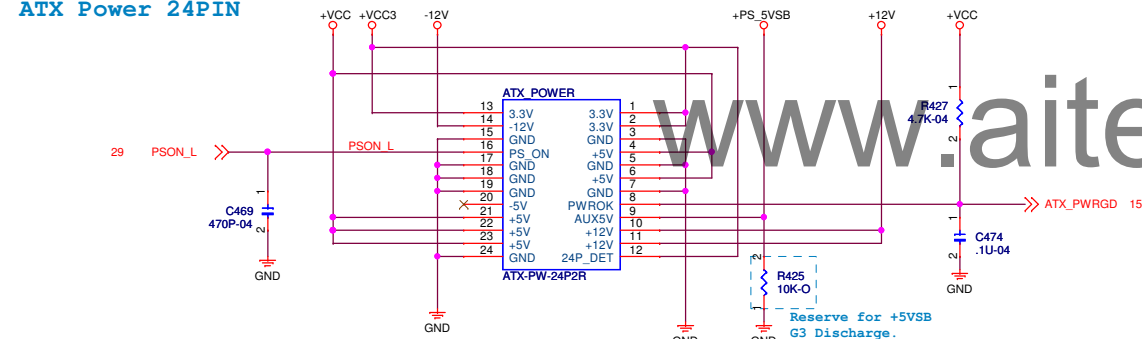
WW23 Intel POR : VCCSA=0.925V for IVY/Sandy Bridge

VCCSA Voltage Selection		
	0.925V	0.85V
CPU (ES1 sample)	stuff A (control by VCCSA_VID)	X
CPU (ES2 sample)	Sandy->VCCSA_VID=0;	
CPU (QS)	Ivy->VCCSA_VID=0;	
	Unstuff A (default)	X

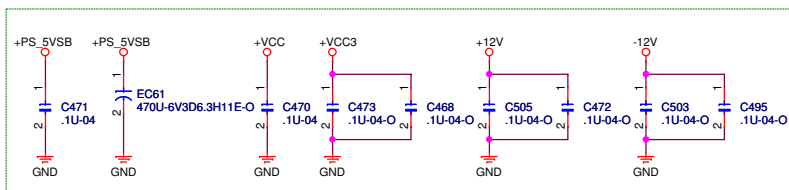


+V_SA

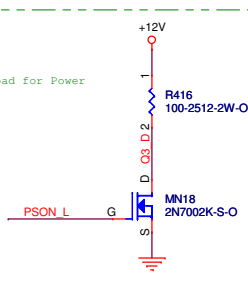
ATX Power 24PIN



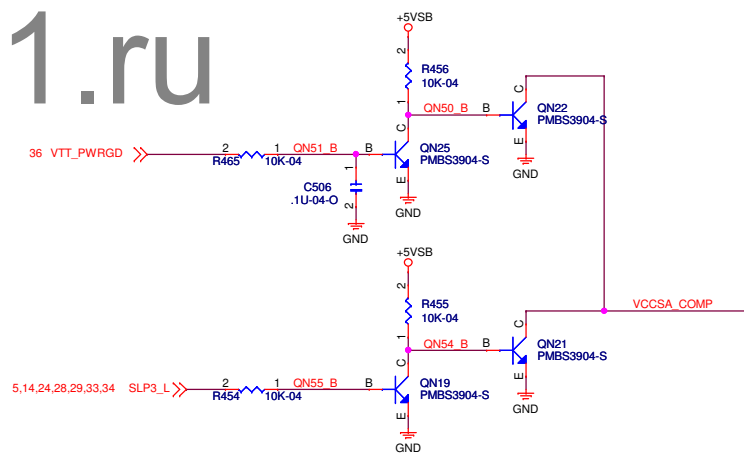
OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5 (CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



Close to ATX PWR CONN



VCCSA Sequence



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Title **DC/DC VCCSA, ATXPWR**

Size Custom Document Number **H61H2-AM3** Rev A

Date: Thursday, March 01, 2012 Sheet 35 of 43

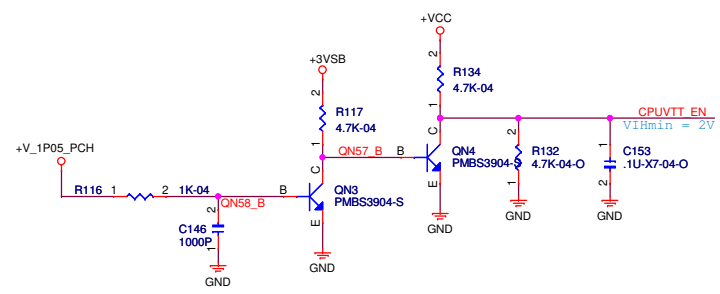


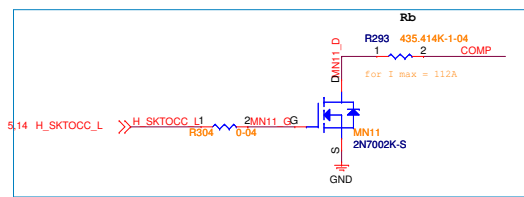
Vout計算公式

VID STATE		RESULT		
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}
1	1	SW0	V _{SET1}	V _{OUT1}
1	0	SW1	V _{SET2}	V _{OUT2}
0	1	SW2	V _{SET3}	V _{OUT3}
0	0	SW3	V _{SET4}	V _{OUT4}

The diagram shows a multi-bit DAC circuit. On the left, a resistor network with resistors R_{FB} , R_{S1} , R_{S2} , R_{S3} , and R_{S4} is connected to a common node. A feedback resistor R_{FB} is connected from the output V_{OUT} to the inverting input of the op-amp. A resistor R_{S5} is connected from the non-inverting input to ground. The op-amp's output V_{COMP} is connected to the V_{REF} input of the DAC block. The DAC block also has a V_{SREF} input, which is connected to a reference voltage source V_{SREF} . The DAC block has four digital inputs, $SW0$, $SW1$, $SW2$, and $SW3$, which are connected to the $D0$, $D1$, $D2$, and $D3$ inputs respectively. The DAC block's output is V_{DAC} , which is connected to the V_{OUT} node. The DAC block is enclosed in a dashed red box.

Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC





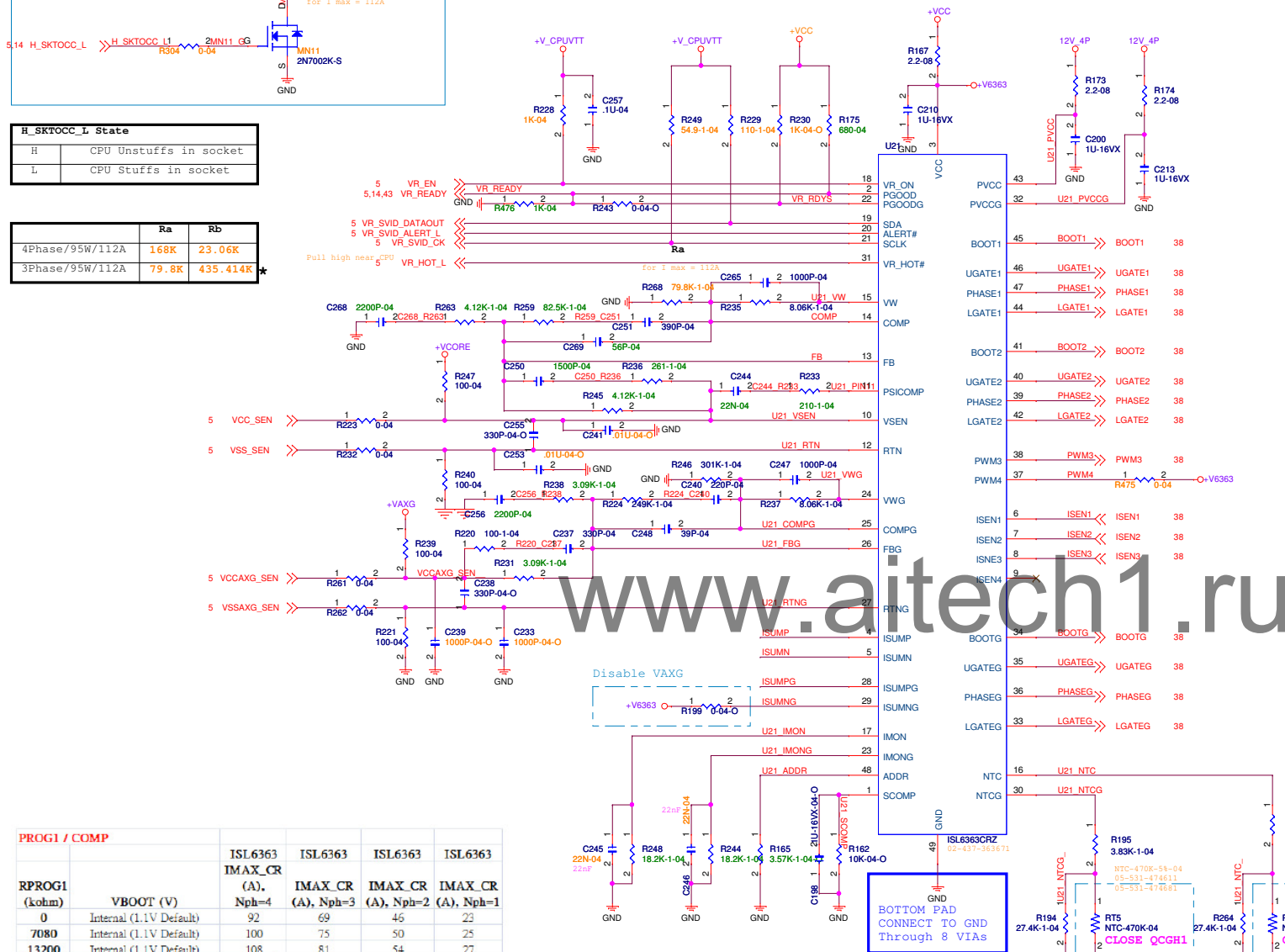
H_SKT0CC_L State	
H	CPU Unstuffs in socket
L	CPU Stuffs in socket

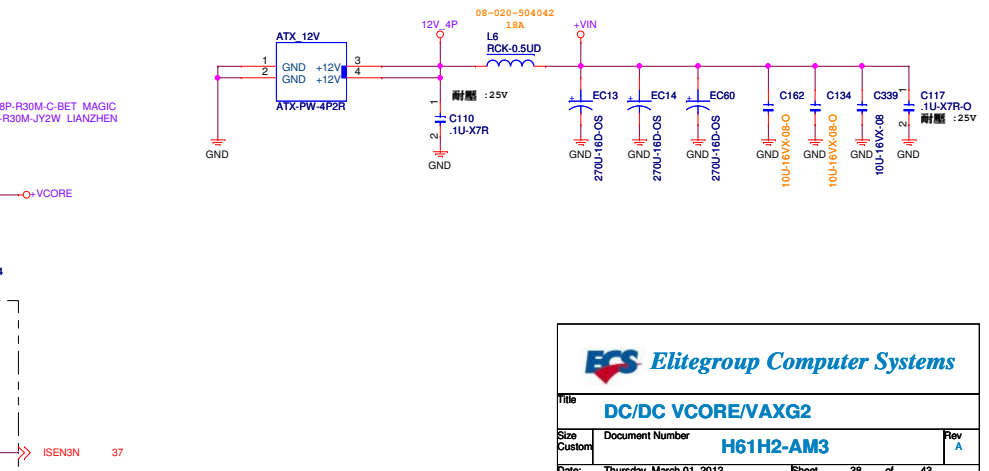
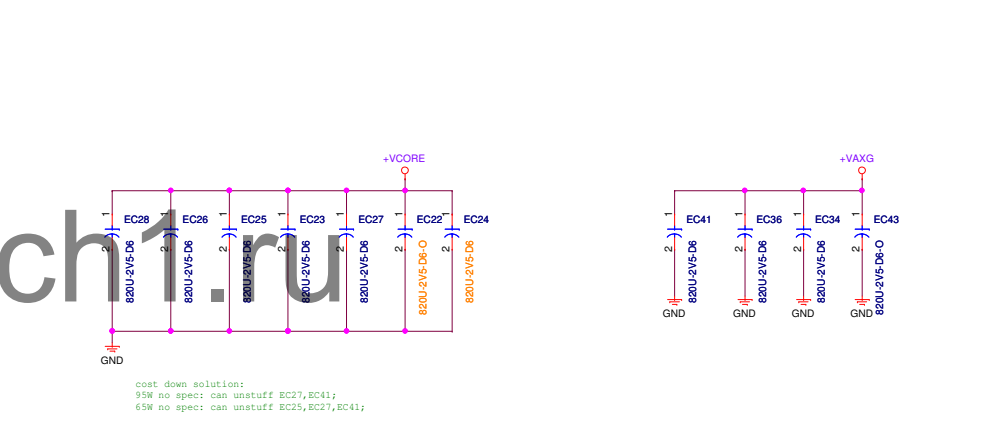
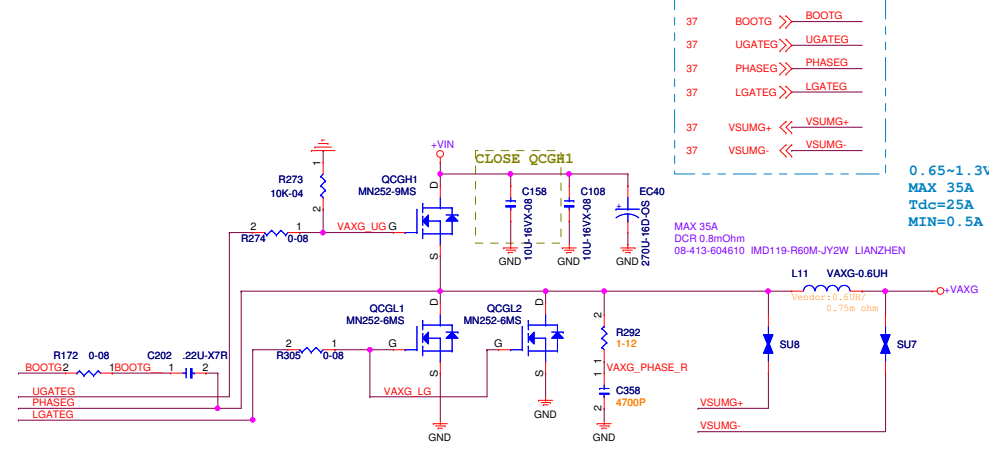
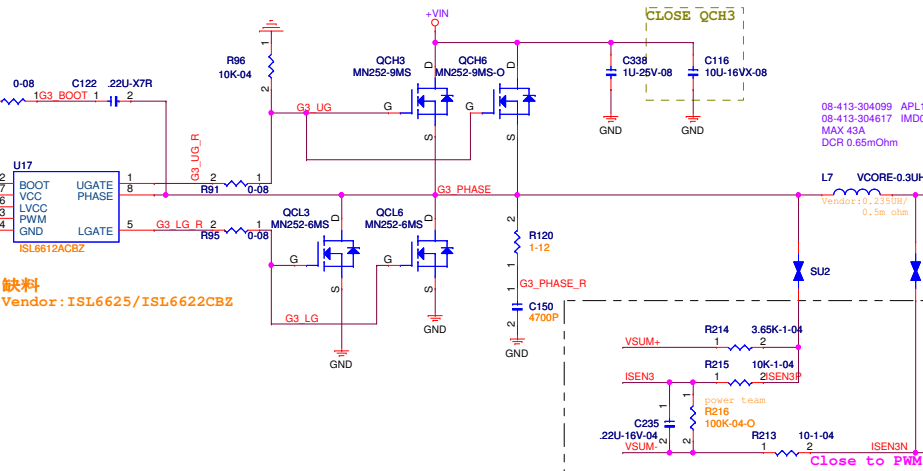
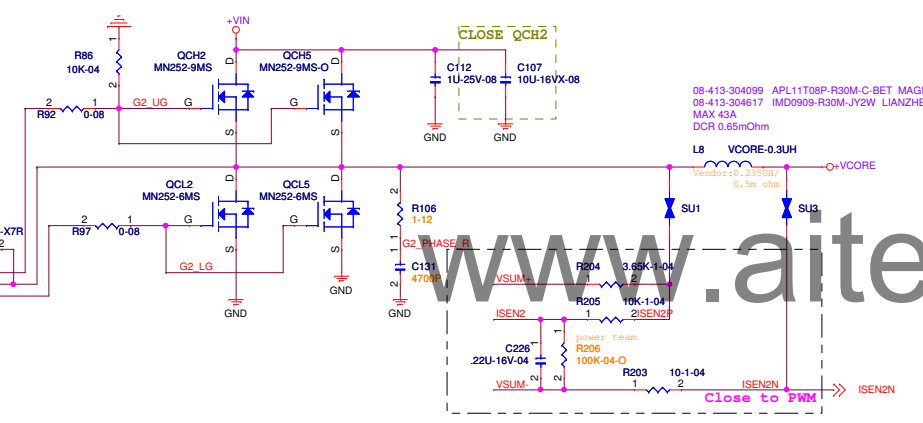
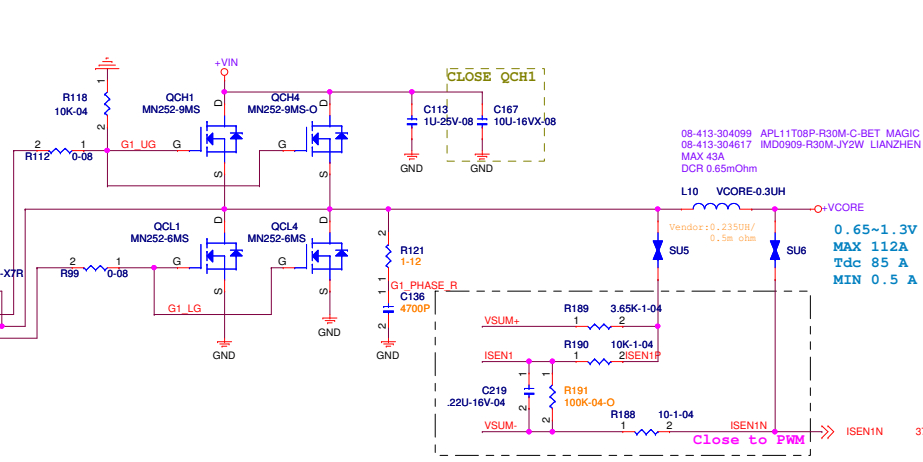
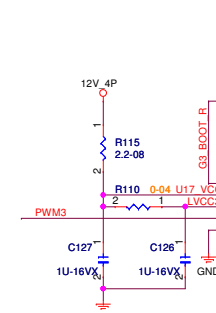
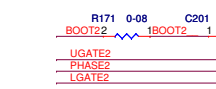
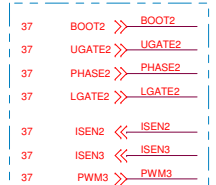
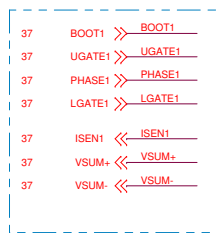
	Ra	Rb
4Phase/95W/112A	168K	23.06K
3Phase/95W/112A	79.8K	435.414K

PROG1 / COMP		ISL6363	ISL6363	ISL6363	ISL6363
RPROG1 (kohm)	VBOOT (V)	IMAX_CR (A), Nph=4	IMAX_CR (A), Nph=3	IMAX_CR (A), Nph=2	IMAX_CR (A), Nph=1
0	Internal (1.1V Default)	92	69	45	23
7080	Internal (1.1V Default)	100	75	50	25
13200	Internal (1.1V Default)	108	81	54	27
20280	Internal (1.1V Default)	116	87	58	29
27120	Internal (1.1V Default)	124	93	62	31
37920	Internal (1.1V Default)	132	99	66	33
51840	Internal (1.1V Default)	140	105	70	35
67440	Internal (1.1V Default)	148	111	74	37
79800	0	148	111	74	37
94440	0	140	105	70	35
114360	0	132	99	66	33
138000	0	124	93	62	31
168000	0	116	87	58	29
198000	0	108	81	54	27
224400	0	100	75	50	25
298800	0	92	69	45	23

TABLE 9. RADDR PROGRAMMING TABLE	
RADDR (kohm)	VR1 and VR1 SV1D Address
3.57	0,1
16.5	2,3
32.4	4,5
59	6,7
88.7	8,9
127	A,B
182	C,D
Open Circuit	0,1

ISL6363CRZ





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File **DC/DC VCORE/VAXG2**

Size Custom Document Number **H61H2-AM3** Rev A

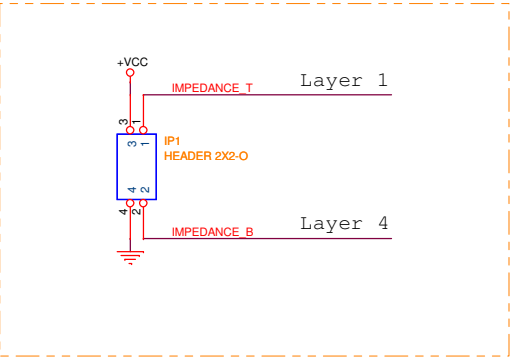
Date: Thursday, March 01, 2012 Sheet 38 of 43

PCH Strap Pin

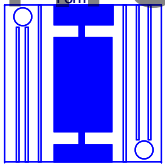
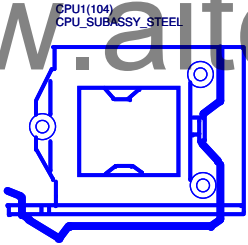
Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down · No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up · intend for Firmware Hub.
GNT[3#]/GPIO[55]	Disable Top-Block Swap	20K internal pull-up · “topblock swap” mode · Disable Need External Pull-up · Integrated 1.05V VRM Enable
INTVRMEN	Enable Integrated 1.05V VRM	20K internal pull-up · The default flash selection is the SPI flash.All
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up · The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
HDA_SDO	Flash Descriptor Security Override/ ME	This signal has a weak internal pull-down.
DF_TV5	Enable DMI termination voltage	The On-Die PLL voltage regulator is enabled
GPIO28	Eable On-Die PLL Voltage Regulator	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.
GPIO15	Enable TLS Confidentiality	

Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/ LRESET#	1 0	Disable Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1 0	Disable K8 power sequence function Enable K8 power sequence function
[JP3,JP5] Pin 124 & Pin 46	FAN_CTL_SE L	Internal VCC-OK	11 10 01 00	The default value of EC Index 63h/6Bh/73h is 80h. The default value of EC Index 63h/6Bh/73h is FFh. The default value of EC Index 63h/6Bh/73h is 00h. The default value of EC Index 63h/6Bh/73h is 40h.



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for 104
special P/N:
20-120-013671
20-120-013672

for 103

X3
JP-W1-P6.25
10-617-002100

20-800-004611

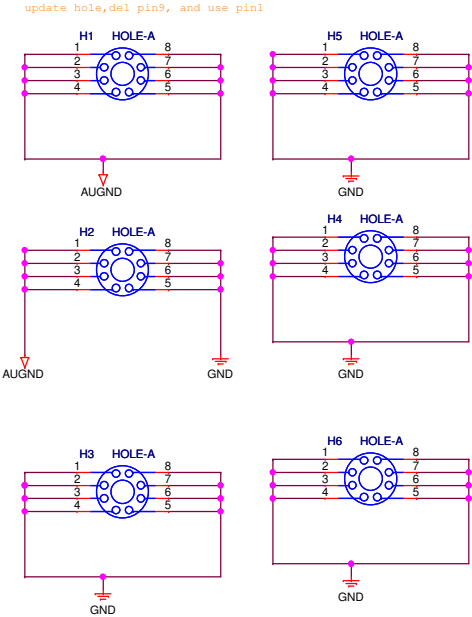
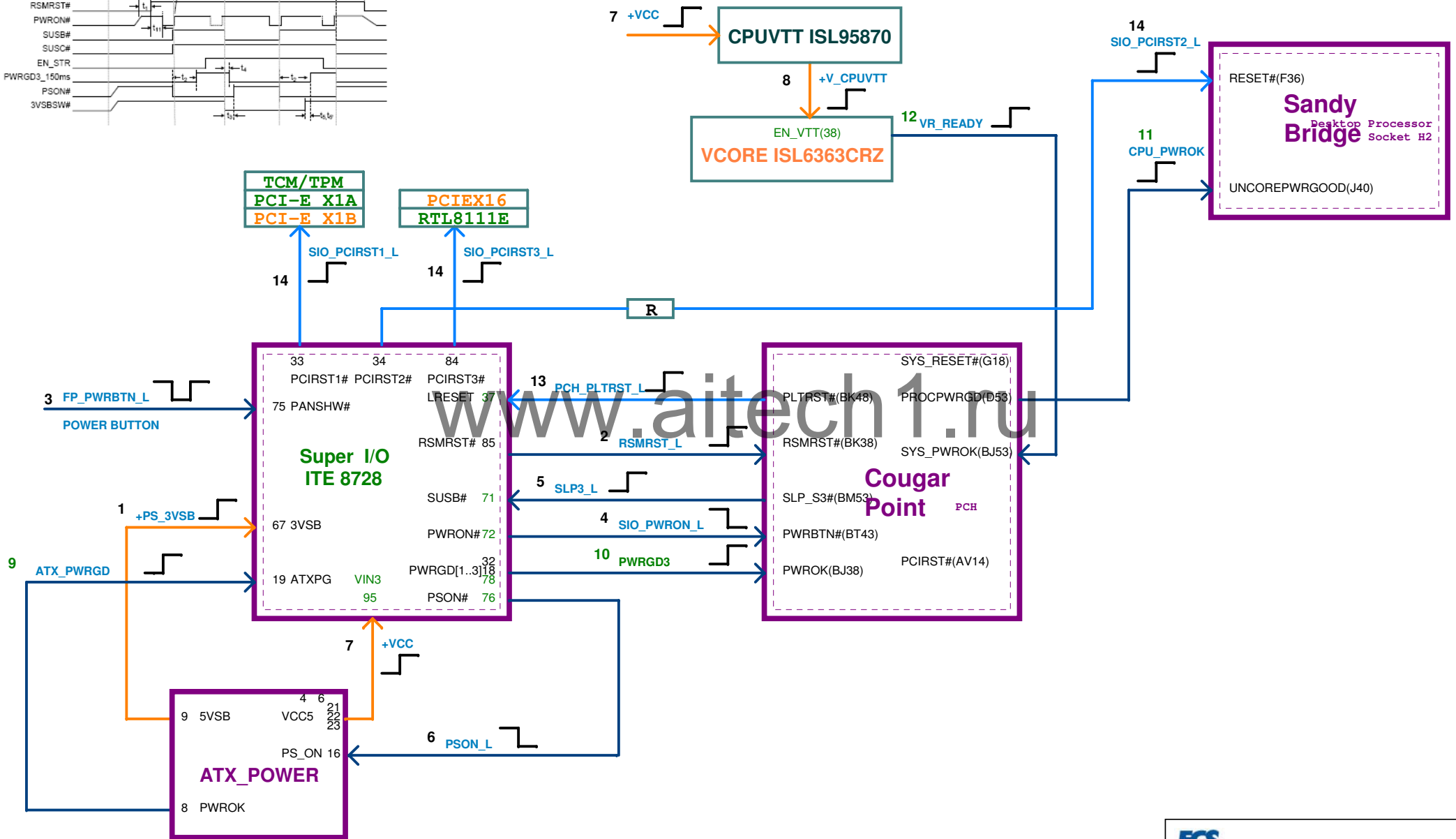
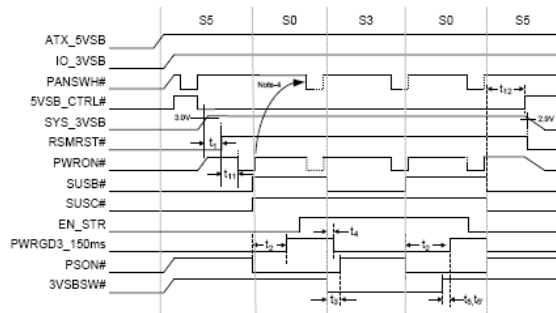


Figure 11-17. EuP Function Signal Timings



NOTE:

Sugar Bay Platform has two clock mode:

1. Integrated Clock Mode (Generate by PCH)

2. Buffer Through Mode (Generate by Clock Gen.)

H61H2-CM use integrated clock mode

